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CAD of Millimeter Wave Frequency Multipliers: An Experimental and Theoretical Investigation of the Heterostructure Barrier Varactor

A Dissertation

Presented to

the Faculty of the School of Engineering and Applied Science

University of Virginia

In Partial Fulfillment

of the Requirements for the Degree of

Doctor of Philosophy (Electrical Engineering)

by

John Robert Jones

January 1996

Approval Sheet

This dissertation is submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy (Electrical Engineering)

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In memory of John Mark Duva, whose dedication to teaching, scientific curiosity, and passion for solving interesting, complex, and diverse engineering problems was an inspiration to all.

Abstract

Prominent applications in the millimeter and submillimeter wavelength regions of the electromagnetic spectrum include atmospheric/oceanic/terrestrial remote sensing, radio astronomy, vehicular sensing and communication, high performance/covert communication, and radiometric imaging under adverse conditions. The availability of light, compact, and reliable solid-state radiation sources at these wavelengths is desirable, but current fundamental solid-state sources have limited maximum frequencies and output powers. Harmonic generation (frequency multiplication) using a nonlinear reactance device is a proven means of achieving higher frequency radiation. Quasi-optical power combining from an array of such devices is an emerging method for achieving higher output powers. With these two techniques in mind, the major goals of this research were (1) the development of accurate and fully self-consistent computer-aided analysis and design techniques for millimeter wave frequency multiplier devices and circuits, and (2) the design, fabrication, and testing of state-of-the-art planar frequency triplers using the Heterostructure Barrier Varactor (HBV), a nonlinear reactance device ideally suited for use in quasi-optical frequency tripler arrays.

In order to effectively design millimeter and submillimeter wave frequency multipliers, both the electrical and thermal properties of the device and circuit must be analyzed in a fully self-consistent manner. To facilitate such an analysis, large-signal time- and temperature-dependent numerical device simulators have been developed for generic GaAs/InGaAs/AlGaAs and InGaAs/InP/InAlAs HBV as well as GaAs and InP Schottky Barrier Varactor (SBV) structures. The numerical device simulators are based on the drift-diffusion equations, and self-consistently combine current transport through the device bulk with current across the abrupt heterointerfaces or metal-semiconductor interface. Given the importance of both the nonlinear device and its embedding circuit, the device simulators have been combined with a novel and efficient harmonic-balance circuit analysis technique. The static thermal properties of whisker-contacted and planar geometry frequency multiplier circuits are used to calculate the average temperature across the active region of the varactor for use in the appropriate device simulator. Excellent correlation has been obtained between the HBV device simulator and experimental d.c. I-V and static C-V

characteristics for several GaAs/AlGaAs and GaAs/InGaAs/AlGaAs HBVs. The combined numerical device/harmonic-balance circuit simulators for both HBVs and SBVs have been compared to published experimental r.f. results, as well as to harmonic-balance results utilizing quasi-static equivalent circuit device models. These comparisons show that significantly improved correlation to experimental data is obtained by using physics-based numerical device models in place of the standard quasi-static equivalent circuit device models.

Prototype planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBVs for tripling from 80 GHz to 240 GHz have been fabricated using a process in which the device "surface channel" is etched prior to the formation of the contact pad-to-anode "finger". Formation of the device "finger" after etching the "surface channel" is facilitated by a trench planarization technique, and yields a device with minimal parasitic capacitances. This process is directly applicable to the fabrication of quasi-optical HBV frequency tripler arrays. Planar four barrier HBV triplers with nominal 10 μm diameter anodes have been tested in a crossed-waveguide tripler block; as much as 2 mW of power has been generated at 252 GHz with a flange-to-flange tripling efficiency of 2.5 %. These devices are the first planar or multi-barrier HBV triplers reported, and their output powers are nearly double that of previous whisker-contacted single barrier HBVs.

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List of Symbols

a	circle radius or lattice constant
b	valance-band deformation potential
c	constant
d_n	complex under-relaxation parameter
f	frequency
h	distance or Planck's constant
i	current
k	Boltzmann's constant or time sweep iteration number
l	length
m^*	electron effective mass
n	electron density
p	Newton-Raphson iteration number
q	electron charge
r	circle radius
t	time or thickness
w	width
v	voltage
x	position
A	area
A^*	current prefactor
$\hat{A}$	nonlinear operator
C	capacitance or Euler's constant
C_{ij}	elastic stiffness constant
D	electric displacement
D_n	electron diffusion coefficient
E_c	conduction-band edge energy
E_g	energy gap
$I, \hat{I}$	current
J_d	electron displacement current density
J_n	electron conduction current density
J_{total}	electron total current density
$\hat{J}$	linear Jacobian matrix
L_D	Debye length
N_c	effective conduction-band density of states
N_D	donor impurity concentration
P	power, tunneling probability, or pressure
R	resistance

S	scaling factor
T	absolute temperature
$V, \tilde{V}$	voltage
V_n	alloy potential
X	reactance
Z	impedance
χ	electron affinity
δ	skin depth
ε	dielectric permittivity
ε_0	permittivity of free space
ϕ_b	barrier height
ϕ_n	electron quasi-Fermi potential
γ	energy gap bowing constant or propagation constant
η	efficiency or ideality factor
κ	thermal conductivity
λ	wavelength
μ_0	permeability of free space
μ_n	electron mobility
π	pi
θ	angle
ρ	resistivity or reflection coefficient
ρ_{oc}	specific contact resistivity
σ	conductivity
τ_p	electron momentum relaxation time
τ_w	electron energy relaxation time
υ	velocity
ω	radian frequency
ξ	electric field
ψ	electrostatic potential
ζ	generic material parameter
Φ_{mwf}	metal work function
$(\partial E_g/\partial P)_T$	bandgap pressure coefficient at a constant temperature
ΔE_c	conduction-band edge energy discontinuity
ΔE_g	energy gap difference
ΔE_v	valence-band edge energy discontinuity
$\Delta\Phi_b$	effective barrier height lowering
Δx_c	critical tunneling width

Chapter 1
Introduction

1.1 Motivation for Research

The millimeter and submillimeter wavelength regions of the electromagnetic spectrum continue to be of interest for advanced scientific, military, and commercial applications. Millimeter waves correspond to frequencies between 30 GHz and 300 GHz while submillimeter waves correspond to frequencies between 300 GHz and 3 THz. Prominent applications at these wavelengths include detection of emission spectra from celestial bodies (radio astronomy)[1.1, 1.2], atmospheric, terrestrial, and oceanic remote sensing[1.3, 1.4], diagnostic techniques for the study of plasma physics[1.5 - 1.7], chemical spectroscopy, vehicular sensing and communication for intelligent cruise control, intelligent traffic control, vehicle-to-roadside communication, and automotive collision avoidance systems[1.8 - 1.11], high performance and/or covert communication[1.8, 1.12], electronic warfare (smart munitions), and radiometric imaging under adverse weather conditions or for contraband detection[1.12]. Although high power vacuum tube and gaseous tube radiation sources are available at these wavelengths, they are hindered by their large size and unreliable operation, and they require a significant amount of support equipment. To fully develop these applications, the availability of light, compact, and reliable solid-state radiation sources at these wavelengths is highly desirable. Current fundamental solid-state sources include an assortment of two-terminal (Josephson oscillators, resonant tunneling devices, transferred-electron devices, and transit-time devices) and three-terminal (MESFETs, HFETs, and HBTs) devices, but all of these devices have rather limited maximum oscillation frequencies and/or output powers. Excellent reviews of the state-of-the-art in vacuum tube, gaseous tube, and solid-state radiation sources at millimeter and submillimeter wavelengths are given in references [1.13] and [1.14].

Given the aforementioned limitations, harmonic generation, or frequency multiplication, using a nonlinear reactance device in series with a fundamental solid-state

source is a proven means of producing higher frequency radiation[1.13]. Additionally, quasi-optical power combining in free space from an array of fundamental sources or frequency multipliers is an emerging method for producing higher output powers and reducing losses associated with the source circuit[1.14 - 1.16]. With these two techniques in mind, the major goals of this research were (1) the development of accurate and fully self-consistent computer-aided analysis and design techniques for millimeter wave frequency multiplier devices and circuits, and (2) the design, fabrication, and testing of state-of-the-art planar frequency triplers using the Heterostructure Barrier Varactor (HBV), a nonlinear reactance device ideally suited for use in quasi-optical frequency tripler arrays.

1.2 Computer-Aided Analysis and Design of Nonlinear Millimeter and Submillimeter Wave Circuits

In order to effectively design highly nonlinear circuits such as large-signal amplifiers, frequency converters such as mixers and multipliers, or oscillators, both the electrical and thermal properties of the active device and its embedding circuit must be analyzed in a fully self-consistent manner. To achieve such a self-consistent analysis, the electrical interaction between the nonlinear active device and its linear embedding circuit is typically determined using a harmonic-balance circuit analysis technique. In this scheme, the active device is usually modeled analytically by a lumped quasi-static equivalent circuit. The use of such an equivalent circuit model for the active device, however, has limited validity at high device operating frequencies and drive levels, requires significant insight into the operation of the active device in order to develop an approximate equivalent circuit topology, and requires a laborious and often non-unique procedure to determine the elements of the equivalent circuit as functions of bias, frequency, and temperature. The validity of such an active device model is particularly suspect at millimeter and submillimeter wavelengths where the large-signal nonstationary high frequency dynamics of carrier transport begin to dominate device operation[1.17 - 1.26].

The analysis and design approach for high frequency nonlinear circuits presented in this dissertation involves the use of a drift-diffusion numerical device model in conjunction with a novel harmonic-balance circuit analysis technique. To date, only limited

attempts have been made to combine physics-based numerical device models with nonlinear circuit analysis techniques such as the harmonic-balance technique[1.27 - 1.29] due to the excessive computational resources and simulation times required. Although the focus here is on millimeter wave HBV and SBV frequency multipliers, this approach is applicable to a wide range of highly nonlinear circuits[1.21, 1.22, 1.30], and can be extended to submillimeter wave frequencies by using a sufficiently sophisticated numerical device model such as a full momentum/energy-balance or Monte-Carlo device model. In general, this approach allows for the careful examination of the internal physical phenomena occurring in a wide array of highly nonlinear active devices. Such insight is important at high frequencies and for devices, particularly novel ones, whose terminal characteristics are not amenable to description via analytical models. Only the general approach presented in this dissertation allows for the accurate and self-consistent modeling of large-signal nonstationary high frequency carrier dynamic effects such as current saturation, the bias-dependent parasitic impedance and shunting capacitance of device undepleted regions, electron velocity saturation, and electron mass-inertial effects[1.17 - 1.26]. It is the belief of the author that analysis and design approaches as advocated in this work are essential to the development of efficient and reliable circuits operating into the terahertz frequency range.

Due to computational demands, the practical realization of this analysis and design approach requires efficient and robust numerical device simulation and harmonic-balance circuit analysis techniques to allow for their synergistic integration. To facilitate a fully self-consistent analysis of HBV and SBV frequency multipliers, large-signal time- and temperature-dependent numerical device simulators, with excellent computational speed and convergence properties, have been developed for generic GaAs/InGaAs/AlGaAs on GaAs and InGaAs/InP/InAlAs on InP HBV and conventional GaAs and InP SBV structures having arbitrary doping profiles. The numerical device simulators are based on the first two moments of the Boltzmann transport equation coupled to Poisson's equation, and combine electron transport through the device bulk with electron transport across the abrupt heterointerfaces or metal-semiconductor interface in a fully self-consistent manner. The device simulators have been combined with a novel and efficient harmonic-balance circuit simulation technique specifically designed to facilitate the inclusion of a numerical

device simulator. The combined numerical device/harmonic-balance circuit simulators provide unified computer-aided design environments for entire HBV or SBV frequency multiplier circuits so that these circuits can be co-designed from both a device and a circuit point of view. Such co-design requires the user to specify the device geometry, doping profile, and alloy composition profile, as well as the parasitic device impedances and embedding impedances of the circuit. In conjunction with the combined numerical device/harmonic-balance circuit analysis, the steady-state thermal properties of whisker-contacted and planar geometry frequency multiplier circuits are analyzed based on the amount of power dissipated in the active region of the device and the thermal resistance to heat flow presented by the various elements that make up the circuit. From these quantities the average temperature across the active region of the varactor can be estimated for use in the appropriate device simulator.

1.3 The Heterostructure Barrier Varactor

The HBV[1], first proposed in 1989[1.31], has received considerable attention[1.32 - 1.40] as a promising device for high efficiency frequency multiplication in the millimeter to submillimeter wavelength range because of its attractive device characteristics and large number of design parameters. A single barrier HBV consists of a large bandgap semiconductor sandwiched between symmetric moderately doped modulation regions of smaller bandgap material (see Figure 1) such that the device has an evenly symmetric nonlinear capacitance-voltage (C-V) relationship about zero d.c. bias. This evenly symmetric device C-V characteristic eliminates the even-harmonic components from the output current waveform so that high efficiency frequency multiplier circuits, which do not require d.c. bias and which require fewer idlers than standard Schottky Barrier Varactor (SBV) multipliers, can be realized. These device characteristics make the HBV an ideal device for use in high order frequency multipliers, broadband frequency multipliers, and quasi-optical tripler arrays. The HBV is ideally suited for use as

1. Although this device was originally called the Quantum Barrier Varactor (QBV) and is often called the Single Barrier Varactor (SBV), it is called the Heterostructure Barrier Varactor (HBV) throughout this work to avoid confusion with the Schottky Barrier Varactor (SBV) and to emphasize the importance of the heterostructure alloy composition and doping profiles in the design and operation of the device.

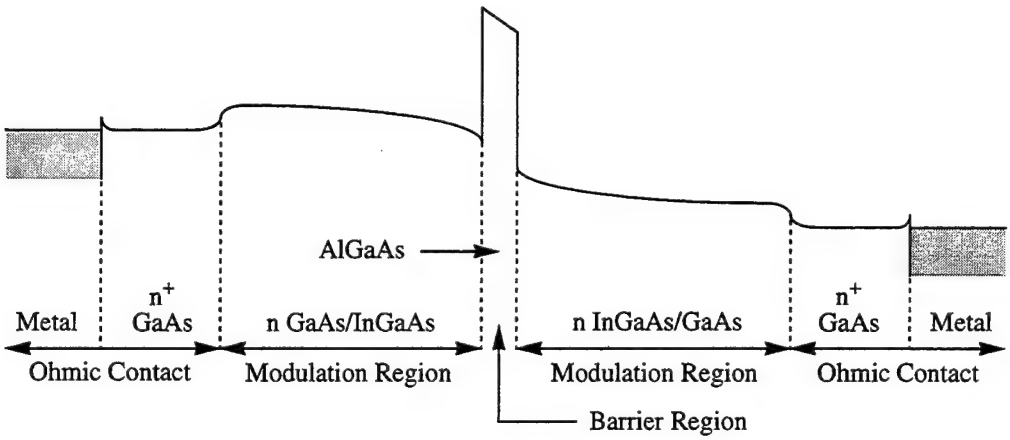

Figure 1.1 One-dimensional schematic diagram, in an illustrative material system, of a Heterostructure Barrier Varactor showing ohmic contact, modulation, and barrier regions.

the multiplier element in a quasi-optical tripler array since no idlers are required for frequency tripling and d.c. bias is not required for the individual elements in the array.

By epitaxially stacking several single barrier HBVs in series, further advantages are obtained including increased device impedances for a given device area, higher device cut-off frequencies for a given device area due to reduced device capacitances, higher power handling capabilities due to the distribution of pump power over several series devices, and increased heat dissipation capabilities for a given capacitance modulation range due to increased device areas. Overall, the HBV has a large degree of design flexibility in that the semiconductor alloy composition and doping profiles, barrier thickness, number of barriers, device geometry, and device area can all be varied. Ultimately, the design flexibility and attractive device characteristics of the HBV suggest that a high efficiency frequency multiplier with excellent device/circuit impedance matching and near-optimum C-V relationship can be achieved with a single device.

1.4 Dissertation Outline

The remainder of this dissertation is organized as follows. Chapter 2 details the electron transport formulation utilized in the HBV and SBV numerical device simulators.

The discretized and normalized transport equations, interface constraints, and boundary constraints required for the time-dependent simulation of both HBVs and SBVs are cataloged in Appendix A along with a detailed description of the Newton-Raphson solution algorithm utilized to solve the resulting two-point boundary value problem. The material parameters required to simulate devices comprised of materials in the GaAs/InGaAs/AlGaAs on GaAs or InGaAs/InP/InAlAs on InP material systems are given in Appendix B. The nonlinear circuit simulation of frequency multipliers is presented in Chapter 3. This chapter details the novel harmonic-balance circuit analysis technique utilized in this work, and outlines the integration of the numerical device simulation and harmonic-balance circuit analysis techniques. A detailed derivation of the novel harmonic-balance circuit analysis algorithm is given in Appendix C, while Appendix D catalogs the d.c. and frequency-dependent parasitic impedance equations, for whisker-contacted geometry HBV and SBV frequency multiplier diodes as well as planar geometry HBV frequency multiplier diodes, required for the harmonic-balance circuit analysis. The static thermal model developed for the analysis of whisker-contacted and planar frequency multiplier circuits is presented in Chapter 4; Appendix E catalogs the thermal resistance expressions utilized in this model for the two circuit geometries. A comparison of experimental d.c. and r.f. results with theoretical results from the numerical device and integrated numerical device/harmonic-balance circuit simulators is made in Chapter 5 for both HBVs and SBVs. A low parasitic fabrication process for planar HBVs is described in Chapter 6; overviews of the whisker-contacted HBV and coplanar waveguide HBV test structure fabrication processes are also given in this chapter. The frequency tripler test setup used in this work is described in Chapter 7, and 80/240 GHz tripler test results are presented for the prototype four barrier planar HBVs described in Chapter 6. Finally, a summary of the present research is given in Chapter 8 along with conclusions and suggestions for future work.

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Chapter 2

Device Simulation of Heterostructure Barrier and Schottky Barrier Varactors

The large number of device design parameters coupled with circuit and thermal constraints makes the task of designing frequency multiplier devices a daunting one. Furthermore, as will be shown in Chapter 5, the accurate analysis and design of millimeter wave frequency multiplier devices requires the use of a physics-based numerical device simulator in order to self-consistently account for such high frequency phenomena as current and drift-velocity saturation[2.1 - 2.10]. With these concerns in mind, temperature-dependent numerical device simulators, with excellent computational speed and convergence properties, have been developed to analyze the d.c. and large-signal time-dependent electrical characteristics of generic heteroepitaxial InGaAs/InAlAs on InP, InGaAs/InP on InP, and GaAs/InGaAs/AlGaAs on GaAs Heterostructure Barrier Varactors (HBVs) as well as homoepitaxial GaAs and InP Schottky Barrier Varactors (SBVs). Although the present focus is on HBVs and SBVs, the general transport formulation/numerical solution technique presented in this chapter is applicable to all unipolar devices having ohmic and/or Schottky contacts, and which contain regions of smoothly varying alloy composition interrupted by a finite number of abrupt material discontinuities.

2.1 Transport Formulation

The general approach to numerical device simulation taken in this dissertation is to self-consistently model carrier transport through the bulk region(s) of a device subject to constraints imposed at heterointerfaces, metal-semiconductor interfaces, and/or ohmic contacts. For HBVs, current transport through the heterostructure bulk is self-consistently combined, therefore, with thermionic and thermionic-field emission current constraints imposed at the heterointerfaces. Likewise, for SBVs, current transport through the device bulk is self-consistently combined with thermionic and thermionic-field emission current

constraints imposed at the metal-semiconductor contact. For the latter device, this simulation approach is analogous to the analytical thermionic-emission/diffusion theory discussed in references [2.11] through [2.13]. The self-consistent inclusion of heterointerface or metal-semiconductor interface boundary constraints will be shown to play a crucial role in the accurate simulation of both of these devices.

2.1.1 Transport in Bulk Regions

Current flow in the bulk active region(s) of an HBV or SBV is essentially one-dimensional and dominated by majority carriers. As such, carrier transport in the bulk region(s) of these devices has been described by a set of coupled nonlinear differential equations for electrons derived from the first two moments of the Boltzmann transport equation, and Poisson's equation. These equations are valid in regions with smoothly varying alloy composition and/or doping profiles, and hydrodynamically model the scattering and diffusive transport mechanisms of electrons within a device subject to a d.c. bias or general time-dependent excitation.

For computational simplicity, nondegenerate carrier statistics and fully ionized dopants are assumed, and conduction-band nonparabolicity and trapped interface charge are not considered. The resulting equations governing d.c. and time-dependent transport are

$$\frac{\partial n(x,t)}{\partial t} = \frac{1}{q}\frac{\partial J_n(x,t)}{\partial x}, \tag{2.1}$$

$$J_n(x,t) = -q\mu_n(x,t)\,n(x,t)\frac{\partial \phi_n(x,t)}{\partial x}, \tag{2.2}$$

and

$$\frac{\partial}{\partial x}\left[\varepsilon(x)\frac{\partial \psi(x,t)}{\partial x}\right] = q\left[n(x,t) - N_D(x)\right], \tag{2.3}$$

where

$$n(x,t) = n_{i,ref} \exp\left[\frac{q}{kT}(\psi(x,t) + V_n(x) - \phi_n(x,t))\right] \tag{2.4}$$

and where J_n is the electron particle current density, n is the electron density, ϕ_n is the electron quasi-Fermi potential, ψ is the electrostatic potential, k is Boltzmann's constant, q is the electron charge, T is the absolute temperature, $n_{i,ref}$ is the intrinsic electron density in the reference material (GaAs or InP), and μ_n, m^*, N_D, and ε are the spatially-dependent electron mobility, electron effective mass, donor impurity concentration, and dielectric permittivity ($\varepsilon = \varepsilon_r \varepsilon_0$ where ε_r is the relative dielectric permittivity and ε_0 is the permittivity of free space), respectively. Since the frequency dependence of the dielectric permittivity is not well established for the semiconductors of interest here, static dielectric permittivity values have been utilized throughout this work.

It is important to note that both field-independent (low field) and field-dependent electron mobilities can be utilized in equation (2.2). For HBVs, field-dependent electron mobilities are not considered since electrons can not reach a steady state with the local electric field in the short high field regions of HBVs, even though the electrons are being heated by the electric field in these regions. For SBVs, both field-independent (low field) and field-dependent mobilities have been utilized, but field-dependent electron mobilities have only been utilized for rather long SBVs such as the UVA 6P4 GaAs SBV. For very short devices or devices operating above about 300 GHz, it becomes imperative to utilize the full momentum-balance and energy-balance equations in place of the drift-diffusion equations presented above so that the electron mobility can vary with the local electron energy or local electron temperature.

Finally, V_n is the spatially-dependent alloy potential, referenced to intrinsic GaAs or InP. This term models the additional electric force, caused by gradients in the electron affinity and the effective conduction-band density of states, that electrons are subjected to in compositionally nonuniform materials[2.14]. The alloy potential, assuming Maxwell-Boltzmann statistics, is given by

$$V_n(x) = \frac{1}{q}[\chi(x) - \chi_{ref}] + \frac{kT}{q}\ln\left[\frac{N_c(x)}{N_{c,ref}}\right] \tag{2.5}$$

where χ and N_c are the spatially-dependent electron affinity and total effective conduction-band density of states, respectively. The total electric field, thus, becomes

$$\xi(x,t) = -\frac{\partial}{\partial x}[\psi(x,t) + V_n(x)] . \tag{2.6}$$

In all, equation (2.1) is the electron particle current continuity equation, equation (2.2) is the electron particle current density equation, and equation (2.3) is Poisson's equation.

2.1.2 Heterointerface Constraints

In order to accurately model the internal physical characteristics of heterostructure devices, careful consideration of carrier transport across abrupt semiconductor material discontinuities is required[2.15, 2.16]. As such, electron transport across the abrupt heterointerfaces of an HBV has been described by a set of nonlinear electron particle current density equations which couple the quasi-Fermi potentials on both sides of the interfaces. Electric displacement continuity, electrostatic potential continuity, and electron particle current density continuity complete the set of interface constraints required for a self-consistent solution at a given heterointerface.

For an HBV biased as shown in Figure 2.1, the electron particle current density constraint at $x = 0$ takes into account thermionic emission and thermionic-field emission (thermally assisted tunneling) of carriers over and through the abrupt barrier, and is derived from an evaluation of the net flux of carriers crossing the heterointerface as given by emission theory and assuming a Maxwell-Boltzmann electron distribution[2.16]. The interface constraints at the $x = 0$ junction are

$$J_n(0,t) = \frac{A^* T^2}{N_c(0^+)} \{\exp\left[\frac{q}{kT}(\phi_n(0^+,t) - \phi_n(0^-,t))\right] - 1\} \exp\left[\frac{\Delta\Phi_b(t)}{kT}\right]$$
$$\times \{n_{i,ref} \exp\left[\frac{q}{kT}(\psi(0,t) + V_n(0^+) - \phi_n(0^+,t))\right]\} , \tag{2.7}$$

$$\varepsilon(0^-)\frac{\partial\psi(0^-,t)}{\partial x} = \varepsilon(0^+)\frac{\partial\psi(0^+,t)}{\partial x} , \tag{2.8}$$

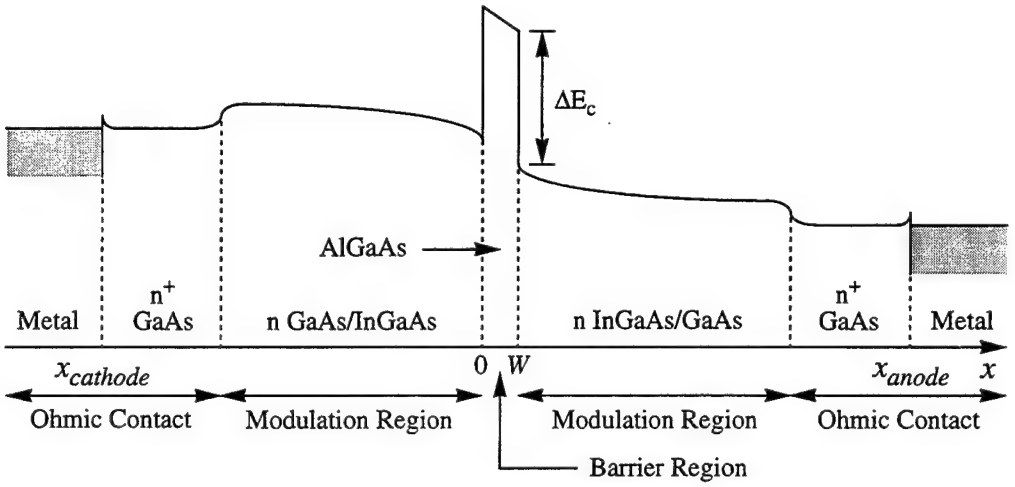

Figure 2.1 One-dimensional schematic diagram, in an illustrative material system, of a Heterostructure Barrier Varactor showing ohmic contact, modulation, and barrier regions.

$$\psi(0^-, t) = \psi(0^+, t) , \tag{2.9}$$

and

$$J_n(0^-, t) = J_n(0^+, t) , \tag{2.10}$$

Coupling of the electrostatic potential, quasi-Fermi potential, and electron particle current density across the heterointerface is evident from these interface constraints. In equation (2.7), A^* is a prefactor analogous to the effective Richardson constant, $\Delta\Phi_b$ is the effective barrier height lowering due to tunneling, and the last term in braces is the electron density on the barrier side of the junction, $n(0^+,t)$. Equation (2.7) can be rewritten, therefore, as

$$J_n(0,t) = q\upsilon_{th}\{\exp\left[\frac{q}{kT}(\phi_n(0^+,t) - \phi_n(0^-,t))\right] - 1\}\exp\left[\frac{q}{kT}\Delta\Phi_b(t)\right]n\left(0^+,t\right) \tag{2.11}$$

where

$$\upsilon_{th} = \frac{A^* T^2}{qN_c(0^+)} \tag{2.12}$$

is one-half of a one-dimensional thermal velocity and $\upsilon_{th}\{\exp\left[\frac{q}{kT}(\phi_n(0^+,t) - \phi_n(0^-,t))\right] - 1\}$ can be interpreted as an effective interface recombination velocity.

At the $x = W$ heterointerface of Figure 2.1, the thermionic emission/thermionic-field emission electron particle current density constraint of equation (2.7) becomes a "fluid-outflow" condition on electron transport. Under such high field conditions, the electron particle current density constraint is, again, derived from an evaluation of the net flux of carriers crossing the heterointerface as given by emission theory, but a drifted-Maxwellian electron distribution is utilized instead of a Maxwell-Boltzmann distribution. The interface constraints at the $x = W$ junction are

$$\begin{aligned} J_n(W,t) &= q\{\langle \upsilon_x \rangle_{R\to L} \exp\left[\frac{q}{kT}(\phi_n(W^-,t) - \phi_n(W^+,t))\right] - \langle \upsilon_x \rangle_{L\to R}\} \\ &\quad \times \{n_{i,ref} \exp\left[\frac{q}{kT}(\psi(W,t) + V_n(W^-) - \phi_n(W^-,t))\right]\} \end{aligned}, \tag{2.13}$$

$$\varepsilon(W^-)\frac{\partial \psi(W^-,t)}{\partial x} = \varepsilon(W^+)\frac{\partial \psi(W^+,t)}{\partial x}, \tag{2.14}$$

$$\psi(W^-,t) = \psi(W^+,t), \tag{2.15}$$

and

$$J_n(W^-,t) = J_n(W^+,t). \tag{2.16}$$

Again, it is evident from these interface constraints that the electrostatic potential, quasi-Fermi potential, and electron particle current density are coupled across the heterointerface. Furthermore, it is important to note that the first term in braces in equation (2.13) can be interpreted as an effective interface recombination velocity while the last term in braces in this equation is the electron density on the barrier side of the junction, $n(W^-,t)$. The left-

and right-directed components of the effective interface recombination velocity are given by, respectively,

$$\langle \upsilon_x \rangle_{R \to L} = \sqrt{\frac{kT}{2\pi m^*_{D\text{-}M}}} \tag{2.17}$$

and

$$\langle \upsilon_x \rangle_{L \to R} = \sqrt{\frac{kT}{2\pi m^*_{D\text{-}M}}} \exp\left[-\upsilon_d^2\left(\frac{m^*_{D\text{-}M}}{2kT}\right)\right] + \frac{1}{2}\upsilon_d\left(1 + \operatorname{erf}\left[\upsilon_d\sqrt{\frac{m^*_{D\text{-}M}}{2kT}}\right]\right) \tag{2.18}$$

where

$$\upsilon_d = \frac{|J_n(W,t)|}{qn(W^-,t)} \tag{2.19}$$

is the displacement of the Maxwellian distribution from equilibrium, and $m^*_{D\text{-}M}$ is a suitable average of the electron effective masses on the two sides of the heterointerface. In all, the interface constraint given by equation (2.13) is the semiconductor-semiconductor heterointerface analog to the boundary constraint of Adams and Tang for metal-semiconductor interfaces at high forward bias when the flat-band condition is exceeded[2.17, 2.18]. Thus, unlike the Adams and Tang result which utilizes the positive portion of a drifted-Maxwellian electron distribution, equation (2.13) is derived assuming a full drifted-Maxwellian electron distribution.

2.1.3 Metal-Semiconductor Interface Boundary Constraints

In a vein similar to that taken for heterostructure devices, careful consideration has been given to carrier transport across metal-semiconductor discontinuities in order to accurately model the internal physical characteristics of devices having Schottky contacts. Electron transport across the metal-semiconductor interface of an SBV has been described, therefore, by a nonlinear electron particle current density equation. In essence, this equation

specifies the electron quasi-Fermi potential on the semiconductor side of the interface based on the amount of current flowing through the device. An expression for the electrostatic potential at the interface, derived using Maxwell-Boltzmann statistics and incorporating a correction term to model image-force lowering, completes the set of interface constraints required for a self-consistent solution at a given metal-semiconductor interface.

The metal-semiconductor interface boundary constraint on the electron particle current density, as derived by Adams and Tang[2.17, 2.18], has been adopted in the present work. Unlike the heterointerface constraint presented in *Section 2.1.2*, this boundary constraint is derived using only the positive portion of a drifted-Maxwellian electron distribution. As such, the backscattering of electrons from the metal has been neglected. The resulting metal-semiconductor electron current density interface constraint at $x = 0$ (see Figure 2.2) is

$$J_n(0,t) = q\upsilon_{rn}\{n_{i,ref}\exp\left[\frac{q}{kT}(\psi(0^+,t) + V_n(0^+) - \phi_n(0^+,t))\right] - n_0\} \tag{2.20}$$

where the first term in brackets is the electron density at the metal-semiconductor interface and n_0 is the equilibrium electron density at this interface. The effective surface recombination velocity for electrons, υ_{rn}, is given by

$$\upsilon_{rn} = \upsilon_d + \sqrt{\frac{2kT}{\pi m^*}}\left\{\frac{\exp\left[-\upsilon_d^2\left(\frac{m^*}{2kT}\right)\right]}{1 + \mathrm{erf}\left[\upsilon_d\sqrt{\frac{m^*}{2kT}}\right]}\right\} \tag{2.21}$$

where m^* is the electron effective mass at the metal-semiconductor interface, and the amount of drift in the electron distribution at the metal-semiconductor interface is modeled as

$$\upsilon_d = \frac{J_n(0,t)}{qn(0^+,t)}. \tag{2.22}$$

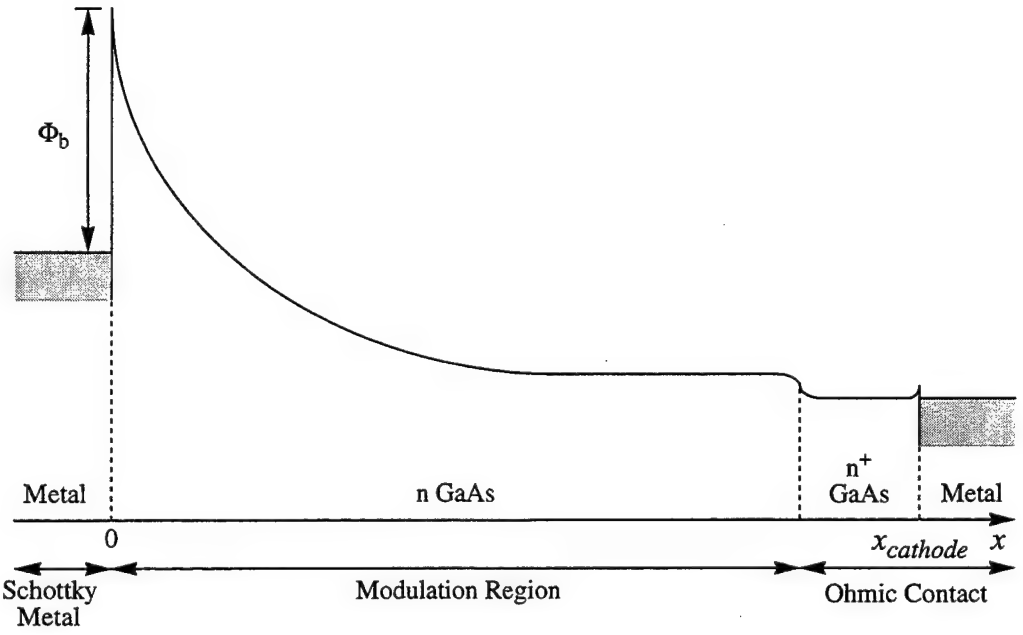

Figure 2.2 One-dimensional schematic diagram, in an illustrative material system, of a Schottky Barrier Varactor showing Schottky metal, modulation, and ohmic contact regions.

The important thing to note about this boundary constraint is the fact that the effective surface recombination velocity is allowed to vary with the electron particle current density crossing the metal-semiconductor interface. As a result of this variation, the use of this boundary constraint precludes the unphysical accumulation of electrons at the Schottky contact when the flat-band condition is exceeded. Such an accumulation of electrons is obtained when the standard electron particle current density boundary constraint of Crowell and Sze[2.11] is utilized since the effective recombination velocity in their formulation is a constant.

The electrostatic potential at the metal-semiconductor interface, assuming the metal is maintained at a potential of zero, is

$$\psi(0) = \frac{\chi_{ref} - \Phi_{mwf}}{q} + \frac{kT}{q}\ln\left(\frac{N_{c,ref}}{n_{i,ref}}\right) \tag{2.23}$$

where χ_{ref} is the electron affinity in the reference material, Φ_{mwf} is the metal work function, and $N_{c,ref}$ is the total effective conduction-band density of states in the reference material. The first term in this equation is the barrier height, Φ_b, at the metal-semiconductor interface divided by the electronic charge. To account for the image-force lowering of the metal-semiconductor barrier, the barrier height is modified by an amount

$$\Delta\Phi_b(t) = \sqrt{\frac{q|\xi(0,t)|}{4\pi\varepsilon(0)}} \tag{2.24}$$

where ξ is the electric field at the metal-semiconductor interface.

2.1.4 *Ohmic Contact Boundary Constraints*

The final boundary of interest in HBVs and SBVs is the ohmic contact where constraints on the electrostatic and electron quasi-Fermi potentials are required. The potentials at such a boundary are derived based on the ideal assumptions of equilibrium and constancy of the electron density at the contact. For HBVs (see Figure 2.1), the resulting boundary constraints on electrostatic and electron quasi-Fermi potentials are

$$\phi_n(x_{cathode}, t) = V_{applied}(t)\,, \tag{2.25}$$

$$\phi_n(x_{anode}) = 0\,, \tag{2.26}$$

$$\psi(x_{cathode}, t) = V_{applied}(t) - V_n(x_{cathode}) + \frac{kT}{q}\ln\left[\frac{N_D(x_{cathode})}{n_{i,ref}}\right], \tag{2.27}$$

and

$$\psi(x_{anode}) = -V_n(x_{anode}) + \frac{kT}{q}\ln\left[\frac{N_D(x_{anode})}{n_{i,ref}}\right], \tag{2.28}$$

where the anode and cathode designation is arbitrary due to device symmetry. For SBVs, the anode is a Schottky contact so that only the cathode ohmic contact equations (equations (2.25) and (2.27)) are utilized (see Figure 2.2). It is important to note that the

electron quasi-Fermi potential on the metal side of the Schottky contact is maintained at zero, in agreement with equation (2.26), so that the polarity of $V_{applied}$ for Schottky diodes is opposite that of standard convention. On the semiconductor side of the Schottky contact the electron quasi-Fermi potential is specified via equation (2.20).

2.1.5 *Tunneling Through Heterointerface Barrier or Metal-Semiconductor Barrier*

Electrons can tunnel through the tip of a heterojunction barrier or metal-semiconductor barrier under appropriate bias conditions, that is at the $x = 0$ heterointerface in Figure 2.1 or the $x = 0$ metal-semiconductor interface in Figure 2.2. Since these tips closely resemble a triangular barrier, the WKB-approximated tunneling probability P decreases exponentially with $(E_T - E)^{3/2}$, where E is the energy of an electron below the energy, E_T, of the tip of the barrier. The number of electrons available for tunneling, however, increases exponentially with $E_T - E$ so that considerable tunneling can occur even when P is very small. For simplicity, tunneling is modeled via an effective barrier height, $E_T - \Delta\Phi_b$, where the barrier height reduction, $\Delta\Phi_b$, is given by[2.19 - 2.21]

$$\Delta\Phi_b(t) = q|\xi(t)|\Delta x_c, \tag{2.29}$$

where ξ is the total electric field in the barrier, and where Δx_c is a fixed critical tunneling width; the electric field dependency of $\Delta\Phi_b$ is self-consistently determined during the numerical simulations. Overall, if the kinetic energy of an electron is greater than $E_T - \Delta\Phi_b$, the barrier is assumed to be completely transparent (P=1); otherwise, the barrier is assumed to be impenetrable (P=0).

The inclusion of tunneling in the heterointerface particle current density expression given by equation (2.7) is facilitated by scaling the electron affinity in the barrier such that a consistent energy band structure is maintained throughout a simulation[2.22]. The alloy potential in the barrier, thus, becomes

$$V_n(x,t) = \frac{1}{q}\left[1 - \frac{\Delta\Phi_b(t)}{\Delta E_c}\right][\chi(x) - \chi_{ref}] + \frac{kT}{q}\ln\left[\frac{N_c(x)}{N_{c,ref}}\right] \tag{2.30}$$

where ΔE_c is the conduction-band edge energy discontinuity as shown in Figure 2.1.

2.2 Numerical Solution Approach

In all, solution of equations (2.1) through (2.3) in the three regions of an HBV or the one region of an SBV, subject to the appropriate boundary constraints and secondary equations, self-consistently treats the coupled effect of electron transport over and through the heterojunction or metal-semiconductor barrier with transport through the bulk region(s) of the device. In order to facilitate the integration of a numerical device simulator for HBVs or SBVs with a harmonic-balance circuit analysis technique, the robust and efficient solution of this boundary value problem is required. As such, careful consideration has been given to the development of a d.c. and large-signal time-dependent simulation scheme with excellent numerical accuracy and convergence properties. Potential problems and inefficiencies associated with the solution technique have been minimized as follows:

1) The electron quasi-Fermi potential is chosen as a state variable instead of the electron density. This provides improved scaling of the Jacobian matrix required for the Newton-Raphson method, and since the magnitudes of potentials do not change by more than an order of magnitude across the entire mesh, superior accuracy control is obtained. In addition, very small currents, down to zero current, can be accurately resolved when the electron particle current density equation is formulated using the electron quasi-Fermi potential as the state variable.

2) The state equations are normalized, using the variable normalization factors given in Table 2.1, such that all first-order derivatives are of comparable magnitude. The normalization factors include two adjustable scaling parameters n_0 and D_0 which are specified by the user. Normalization of the state equations improves the conditioning of the Jacobian matrix required for the Newton-Raphson method.

3) A finely subdivided, nonuniform mesh is utilized for improved accuracy of the numerical results. For HBVs, it is important to note that by allowing the electron quasi-Fermi potential to be discontinuous across the heterointerfaces, as dictated by equations (2.7) and (2.13), the number of mesh points required to resolve the heterointerface regions is reduced considerably.

4) Poisson's equation (equation (2.3)) is reduced to the two first-order differential equations

Table 2.1 Variable Normalizations.

Variables	Normalization Factor
Charge Density (n, $n_{i,ref}$, N_D, N_c)	n_0
Potential (ψ, ϕ_n, V_n, χ/q, Φ/q)	$V_{th} = kT/q$
Position, Distance (x, h)	$L_D = \sqrt{\varepsilon_{r,ref}\varepsilon_0 V_{th}/qn_0}$
Dielectric Permittivity (ε)	$\varepsilon_{r,ref}\varepsilon_0$
Electric Field (ξ)	V_{th}/L_D
Electron Diffusion Coefficient (D_n)	D_0
Electron Mobility (μ_n)	D_0/V_{th}
Current Density (J_n, J_D, J_{total})	qn_0D_0/L_D
Velocity (υ_{th}, υ_x, υ_d, υ_{rn})	D_0/L_D
Frequency (f, ω)	D_0/L_D^2
Time (t,τ_p,τ_w)	L_D^2/D_0

$$D(x,t) = \varepsilon(x)\frac{\partial\psi(x,t)}{\partial x}, \tag{2.31}$$

and

$$\frac{\partial D(x,t)}{\partial x} = q[n(x,t) - N_D(x)] \tag{2.32}$$

where the new state variable D is the electric displacement. As a result of this reduction, an exact Jacobian matrix can be formulated, that is, a Jacobian matrix that includes terms arising from the derivatives of the electron mobility and barrier height lowering parameters with respect to the electric field.

5) To insure robust time-dependent simulations, the right-hand side of equation (2.1) is discretized using a fully implicit (backward Euler) finite-difference temporal discretization scheme. For d.c. simulations, the right-hand side of this equation reduces to zero emphasizing the required constancy of the electron particle current density as a function of position in the device. For time-dependent simulations, the total current density is taken to be the sum of the electron particle current density (J_n) and the displacement current density (J_D)

$$J_{total}(t) = J_D(x,t) + J_n(x,t) \tag{2.33}$$

where the displacement current density is given by

$$J_D(x,t) = \frac{\partial D(x,t)}{\partial t}. \tag{2.34}$$

For simulation purposes, the displacement current density is obtained from the state variables by calculating the change in the electric displacement with respect to the simulation time step.

6) Electric field-dependent electron mobilities are only utilized for time-dependent simulations. In order to simplify the numerical solution algorithm for such simulations, the explicit time-dependence of the electron mobility in equation (2.2) is neglected. As such, the spatially-dependent electron mobilities are held constant for solution at a given time step and are only updated prior to the next time step using the electric field spatial profile from the previous time step. This approach is generally valid since the time scales associated with the electron mobility are significantly larger than the simulation time scale required to obtain acceptable error and convergence properties[2.23].

7) In order to utilize existing numerical codes which solve two-point boundary value problems, all heterointerface constraints are mapped onto two boundary points by appropriately "folding/translating" portions of the device domain and rescaling the transport equations in these regions[2.22]. For a single barrier HBV, this means "folding," at the heterointerfaces, the barrier region back onto the first modulation region, and "translating" the second modulation region onto the first modulation region. This mapping procedure is shown schematically in Figure 2.3. Unfortunately, this technique triples the number of equations to be solved since separate solution of the transport equations is now required in each of the regions (one barrier and two modulation) of an HBV. In addition, careful mesh construction is required since the mesh structure of the first modulation region is imposed on the barrier and second modulation regions.

Overall, equations (2.1), (2.2), (2.31), and (2.32) yield the state variable set J_n, ϕ_n, ψ, and D. For HBVs, after "folding/translating" of the device domain, twelve carrier transport equations must be solved at each mesh point and at a given bias value subject to the heterointerface constraints and the ideal ohmic contact boundary constraints. Likewise, for SBVs, four carrier transport equations must be solved at each mesh point and at a given bias

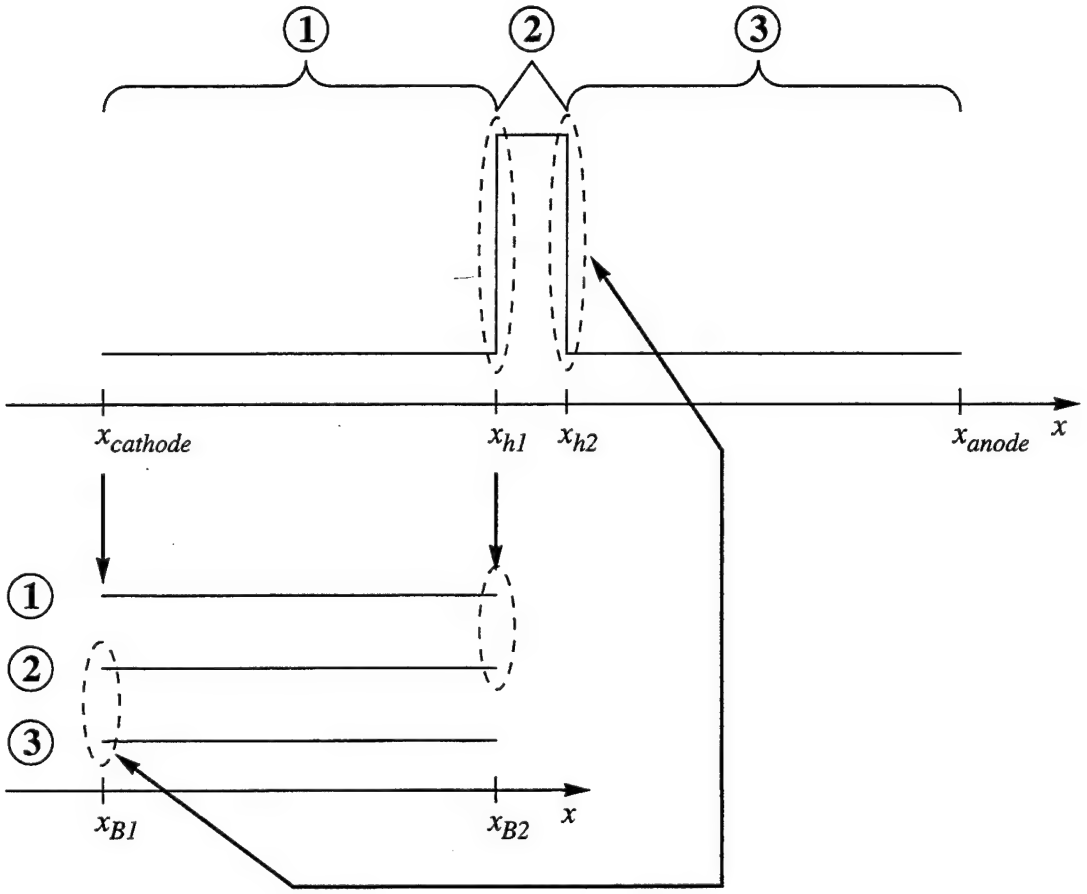

Figure 2.3 Schematic representation of the HBV device domain mapping procedure required for the utilization of existing numerical codes that solve two-point boundary value problems.

value subject to the metal-semiconductor interface boundary constraints and the ideal ohmic contact boundary constraints.

The numerical solution of the resulting boundary value problem is carried out in two steps. First, the thermal equilibrium values of the state variables are obtained from the discretized nonlinear Poisson's equation using a globally convergent nonlinear iterative technique[2.24]. The carrier transport equations are then solved at a given bias value via the coupled-equation Newton-Raphson method. For the initial bias value, the thermal equilibrium solution serves as the starting point for the Newton-Raphson method; for subsequent bias values, the previous solution serves as the starting point. This procedure is very important since good initial conditions are required for reliable convergence of the

Newton-Raphson method, and initial conditions derived from analytical approximations are not readily available for complex heterostructures or metal-semiconductor structures (δ-doped SBVs, for example). In the implementation of the Newton-Raphson method utilized for this work, an exact Jacobian operator is formulated from the continuous system of coupled nonlinear transport equations. The resulting linearized system of equations is then spatially discretized using a trapezoidal-rule finite-difference scheme over a nonuniform mesh and solved by LU decomposition. In order to enhance the convergence range of the method, the Newton-Raphson correction vectors are damped. The normalized time-dependent state equations and boundary constraints for both HBVs and SBVs are given in Appendix A along with a detailed discussion of the finite-difference discretization scheme and the Newton-Raphson solution technique used in this dissertation.

In order to derive an entire d.c. current-voltage (I-V) curve or time-domain current waveform, as well as to obtain information about the internal physics of a given device as a function of bias, the d.c. or time-dependent bias is incrementally changed from the zero bias or initial condition. At each bias value or time step, Newton-Raphson iterations continue until the maximum change in the electron quasi-Fermi and electrostatic potentials across the entire mesh is less than $10^{-6}\ kT/q$ at 300 K. A typical bias-point solution is obtained, with this level of convergence and over a mesh containing approximately 500 grid points, in 3 to 5 Newton-Raphson iterations using a typical voltage increment of 0.01 V. On a Hewlett-Packard Apollo 9000 Series 735 workstation, this corresponds to an average execution time of about two seconds in real (wall) time.

Finally, multiple barrier HBVs are modeled in an ideal fashion by assuming that the barriers are decoupled (the modulation layers are several thousand angstroms in length) and that the terminal voltage is equally divided among the equivalent series-cascaded single barrier HBVs. Therefore, in the simulator, only one single barrier HBV structure is simulated with a terminal voltage equal to the total terminal voltage divided by the number of barriers.

Table 2.2 Low field electron mobility values for the specific materials, ternary compound compositions, and doping concentrations used in this work.

	Electron Mobility ($cm^2/V{\cdot}s$)	
N_D (cm^{-3})	GaAs	$In_{0.0\text{-}0.2}Ga_{1.0\text{-}0.8}As$
$3.5x10^{16}$	4950	—
$8.0x10^{16}$	4375	4375
$1.0x10^{17}$	4200	4200

2.3 Material Parameters

The material systems of interest in this work are heteroepitaxial $GaAs/In_xGa_{1-x}As/Al_xGa_{1-x}As$ on GaAs and $In_xGa_{1-x}As/In_xAl_{1-x}As/InP$ on InP for HBVs, and homoepitaxial GaAs and InP for SBVs. Relevant details about the temperature- and composition-dependent material parameters required for device simulation are given in Appendix B for GaAs, $In_xGa_{1-x}As$, $Al_xGa_{1-x}As$, $In_xAl_{1-x}As$, and InP. Table 2.2 lists the low field electron mobility values used in this work for the materials, ternary compound compositions, and doping concentrations of interest, while Figure 2.4 shows the field- and temperature-dependent electron mobility for n-type ($3.5x10^{16}$ cm^{-3}) GaAs used for the UVA 6P4 SBV simulations of Chapter 5. The field- and temperature-dependent electron mobilities have been obtained from three-valley Monte Carlo simulations under static, uniform electric field conditions based on the work in references [2.25] through [2.28]. The low field electron mobility values for $Al_xGa_{1-x}As$ have been estimated using the technique of reference [2.29] where the electron mobility is a weighted average of the Γ-valley and X-valley mobilities

$$\mu_{n,Al(x)Ga(1-x)As} = \mu_\Gamma f_\Gamma + \mu_X (1 - f_\Gamma) \; . \tag{2.35}$$

The weighting factor f_Γ is the fraction of electrons in the Γ-valley and is given by

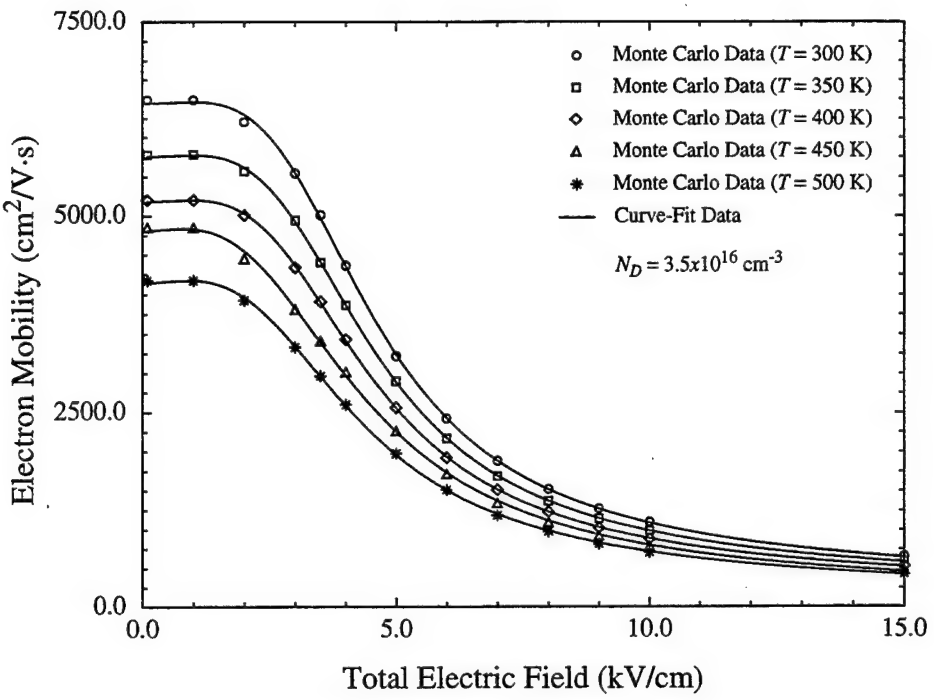

Figure 2.4 Field- and temperature-dependent electron mobilities, for *n*-type ($3.5x10^{16}$ cm^{-3}) GaAs, derived from three-valley Monte Carlo simulations and used for the UVA 6P4 SBV simulations of Chapter 5.

$$f_\Gamma = \frac{n_\Gamma}{n_\Gamma + n_X} = \frac{1}{1 + \left(\frac{m^*_{X,\,Al(x)\,Ga(1-x)\,As}}{m^*_{\Gamma,\,Al(x)\,Ga(1-x)\,As}}\right)^{3/2} \exp\left[\frac{E^\Gamma_{g,\,Al(x)\,Ga(1-x)\,As} - E^X_{g,\,Al(x)\,Ga(1-x)\,As}}{kT}\right]}. \qquad (2.36)$$

For intrinsic $Al_{0.7}Ga_{0.3}As$ ($Al_{0.4}Ga_{0.6}As$), the Γ-valley, X-valley, and total electron mobilities were estimated to be approximately 1786 $cm^2/V{\cdot}s$ (2965 $cm^2/V{\cdot}s$), 231 $cm^2/V{\cdot}s$ (248 $cm^2/V{\cdot}s$), and 231 $cm^2/V{\cdot}s$ (666 $cm^2/V{\cdot}s$), respectively. Other important material parameters including A^* and $m^*_{D\text{-}M}$ will be outlined, as needed, in the appropriate sections of the dissertation.

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Chapter 3

Nonlinear Circuit Simulation of Frequency Multipliers

The performance of a frequency multiplier devices is intimately linked to the circuitry in which it is embedded, particularly at millimeter and submillimeter wavelengths. As such, the design of these devices requires an efficient computer-aided design tool that calculates the terminal characteristics of the nonlinear active device at a sufficient number of harmonics and as a function of the physical characteristics of the intrinsic device, the impedances of the embedding circuit, and the device parasitic impedances. In order to accurately account for the nonlinear interaction between the active device and its embedding circuit, a nonlinear circuit analysis technique is required. Likewise, to accurately calculate the large-signal time-dependent behavior of the intrinsic active device, a numerical simulation of the charge carrier transport in the device should be used. In an effort to avoid exorbitant computational requirements, however, present nonlinear circuit analysis techniques[3.1 - 3.8] require that the active device be represented by a quasi-static equivalent circuit model employing approximate analytical expressions for the circuit elements, or by a "power-series" model in which the device terminal characteristics are given by approximate analytical equations. This approach has been successful for the design of relatively low frequency (< 100 GHz) circuits, and has been a critical factor in the development of monolithic microwave integrated circuits. At higher frequencies, however, such a device model is not sufficiently accurate. Furthermore, significant insight into the operation of the active device is required in order to develop an approximate equivalent circuit topology, and a laborious and often non-unique procedure is required to determine the "power-series" relationships or the elements of the equivalent circuit as functions of bias, frequency, and temperature.

The most prominent nonlinear circuit analysis technique is the harmonic-balance method[3.2, 3.4, 3.5, 3.8]. In this method, the nonlinear circuit is partitioned into a linear multiport subcircuit which is analyzed in the frequency-domain and a nonlinear multiport

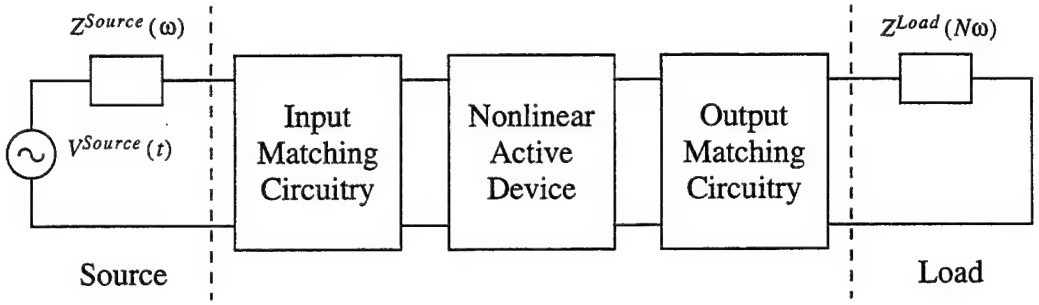

Figure 3.1 Schematic representation of a general nonlinear two-port component showing the nonlinear active device, the source and load impedances, and the embedding circuitry.

subcircuit which is analyzed in the time-domain. Figure 3.2 shows a generalized schematic of this partitioning scheme for the general nonlinear two-port component of Figure 3.1. A finite number of harmonic current or voltage phasors are then balanced between the linear and nonlinear subcircuits; a Fourier transform of the nonlinear subcircuit's time-domain response facilitates a comparison of the two subcircuit responses in the frequency-domain. This nonlinear circuit analysis method is particularly advantageous for circuits operating in the microwave through submillimeter wavelength range since the distributed and dispersive nature of the circuit elements is more readily modeled in the frequency domain. Furthermore, the method can be formulated such that linear subcircuits of any size or those having elements with widely varying time constants can be efficiently analyzed[3.2, 3.4, 3.5, 3.8].

Given the interest in combining physics-based numerical device simulation and nonlinear circuit analysis techniques, and the prominence of the harmonic-balance method, this chapter reviews a novel fixed-point iterative harmonic-balance circuit analysis method[3.9] which can be efficiently integrated with numerical device simulators. To this end, the HBV and SBV frequency multiplier numerical device simulators described in Chapter 2 have been successfully integrated with this harmonic-balance circuit analysis technique. The combined numerical device/harmonic-balance circuit simulators provide unified computer-aided design environments for entire HBV or SBV frequency multiplier circuits so that these circuits can be co-designed from both a device and a circuit point of

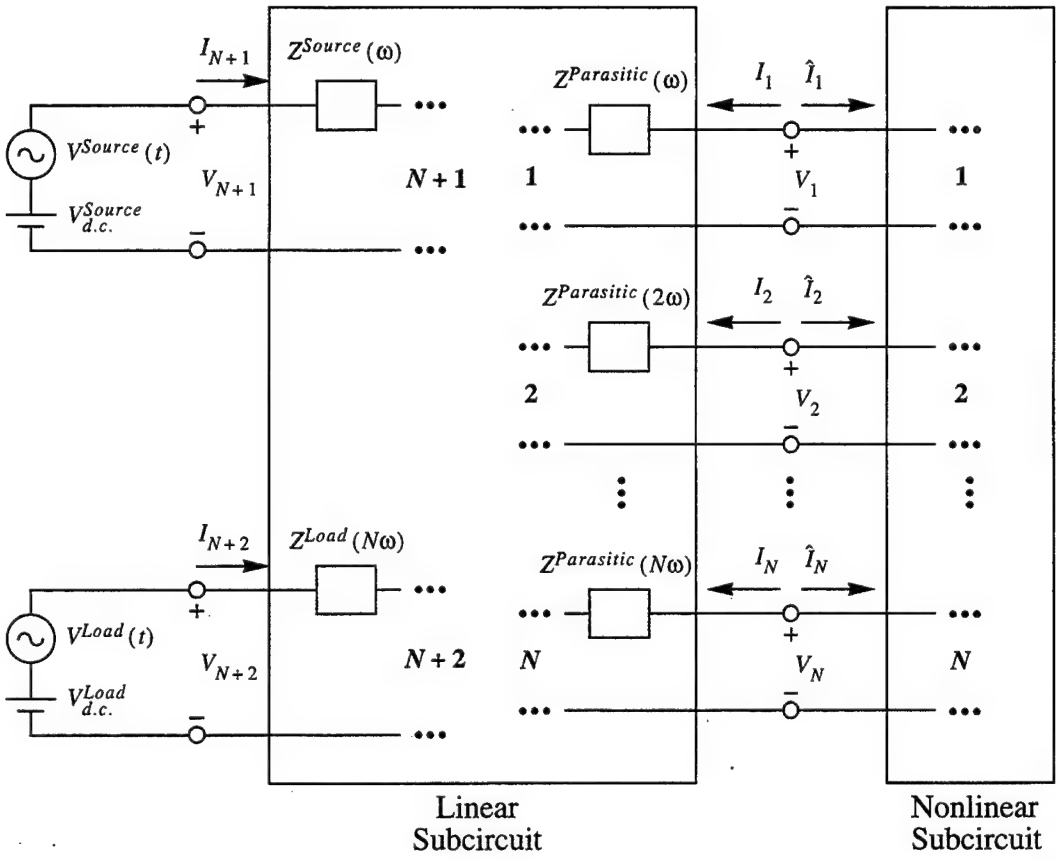

Figure 3.2 Generalized partitioning scheme for separating the nonlinear two-port component of Figure 3.1 into linear and nonlinear subcircuits. Note that the source ($Z^{Source}(\omega)$), load ($Z^{Load}(N\omega)$), and active device parasitic ($Z^{Parasitic}(n\omega)$) impedances have been absorbed into the linear subcircuit, and that, for complete generality, both the input ($N+1$) and output ($N+2$) ports have d.c. and sinusoidal sources.

view. Such co-design requires the user to specify the device geometry, doping profile, and alloy composition profile, as well as the parasitic device impedances and impedances of the embedding circuit.

3.1 Overview of Harmonic-Balance Circuit Analysis Solution Algorithms

There are three general numerical solution techniques for the harmonic-balance analysis of nonlinear circuits, Newton-Raphson based methods, optimization schemes, and

relaxation methods. Excellent reviews of these solution techniques can be found in references [3.1], [3.4], [3.7], and [3.8]. Although Newton-Raphson based methods are the most commonly used harmonic-balance solution algorithms[3.2, 3.4, 3.5, 3.8], they require an initial estimate of the solution that is sufficiently close to the final solution in order to achieve convergence, and they require the calculation, either numerically or analytically, of Jacobian matrices which are typically very large. The required computer resources and computation times for these methods can be, therefore, quite substantial, particularly when the requirements for the storage and manipulation of the Jacobian matrices are considered. Optimization solution methods, like Newton-Raphson based methods, also suffer from the need for repetitive derivative calculations. Furthermore, optimization schemes are relatively slow and inefficient, and they may have convergence problems[3.4, 3.8]. With these disadvantages in mind, the relaxation methods are the ideal solution methods for circuit analyses in which the nonlinear active device is described by a numerical device simulator. Overall, the relaxation methods avoid the repetitive derivative calculations which characterize the optimization and Newton-Raphson based methods, and they do not require an initial estimate of the solution, making them attractive for use in general purpose nonlinear circuit analysis programs.

The novel harmonic-balance circuit analysis technique employed in this work is a relaxation method derived from the Multiple-Reflection (MR) algorithm[3.10, 3.11]. The circuit partitioning scheme for the MR algorithm, shown schematically in Figure 3.3, is characterized by the insertion of a set of fictitious lossless transmission lines between the respective ports of the linear and nonlinear subcircuits. By making the transmission lines an integral number of wavelengths long at the fundamental frequency, and hence at the harmonics of the fundamental frequency, the steady-state waves of the modified circuit will be the same as those of the original circuit. By making the transmission lines electrically long, this partitioning scheme separates the nonlinear circuit analysis into two alternating *steady-state* analyses, one between the linear subcircuit and the transmission lines in the frequency-domain, and one between the nonlinear subcircuit and the transmission lines in the time-domain. Furthermore, this partitioning scheme allows for the use of incident (positive-travelling, V^+) and reflected (negative-travelling, V^-) harmonic voltages waves, composed of linear combinations of the total harmonic voltages and currents at the

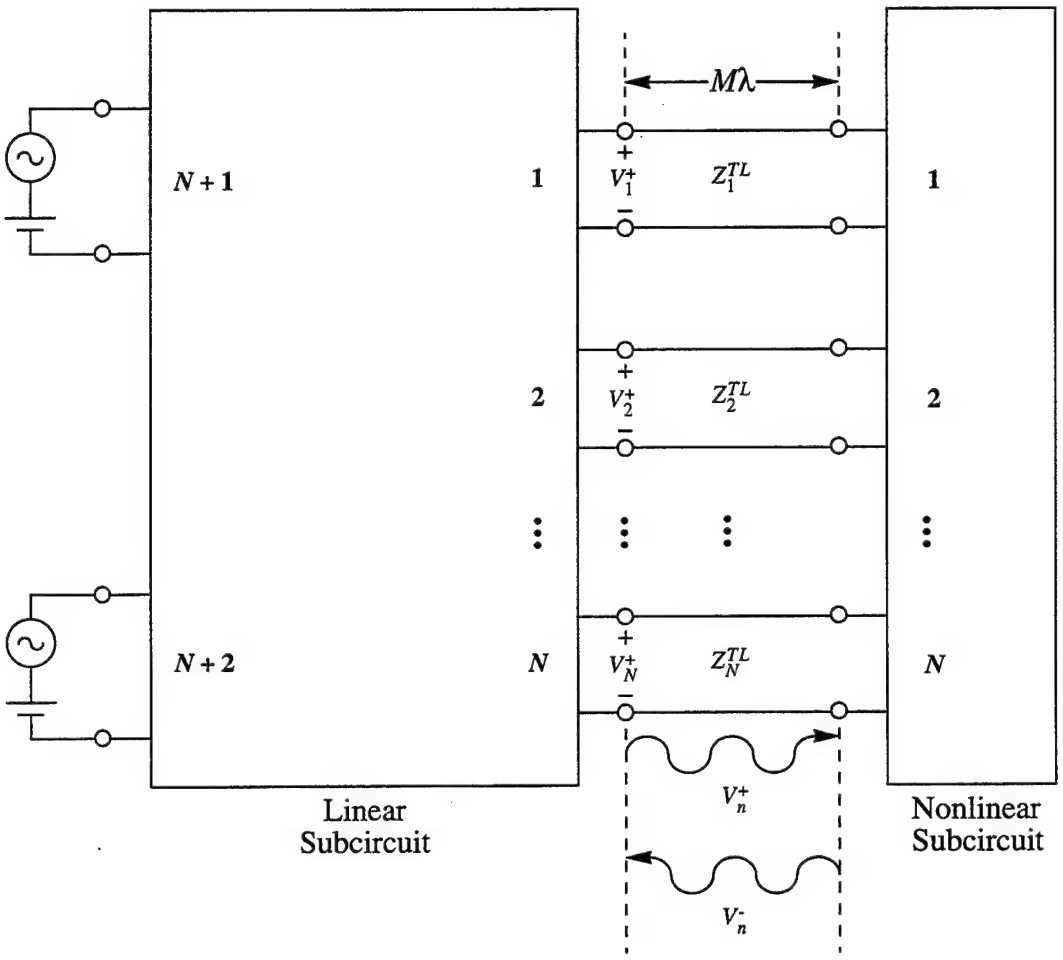

Figure 3.3 Generalized partitioning scheme for separating the nonlinear two-port component of Figure 3.1 into linear and nonlinear subcircuits using fictitious ideal and electrically long transmission lines for analysis via the MR algorithm.

terminals of the nonlinear subcircuit, as the state variables in the nonlinear circuit analysis. Since this choice of state variables takes advantage of the subunitary nature of circuit reflection coefficients, the MR algorithm has fairly robust convergence properties.

Unfortunately, the MR time-domain analysis of the nonlinear subcircuit requires that twice the harmonic voltage wave incident on this subcircuit be sourced through an impedance equal to the characteristic impedance of the fictitious transmission line, Z_n^{TL}, at the harmonic of interest (see Figure 3.4). Hence, the total harmonic voltage across the terminals of the intrinsic device, necessary for numerical or analytical device simulation,

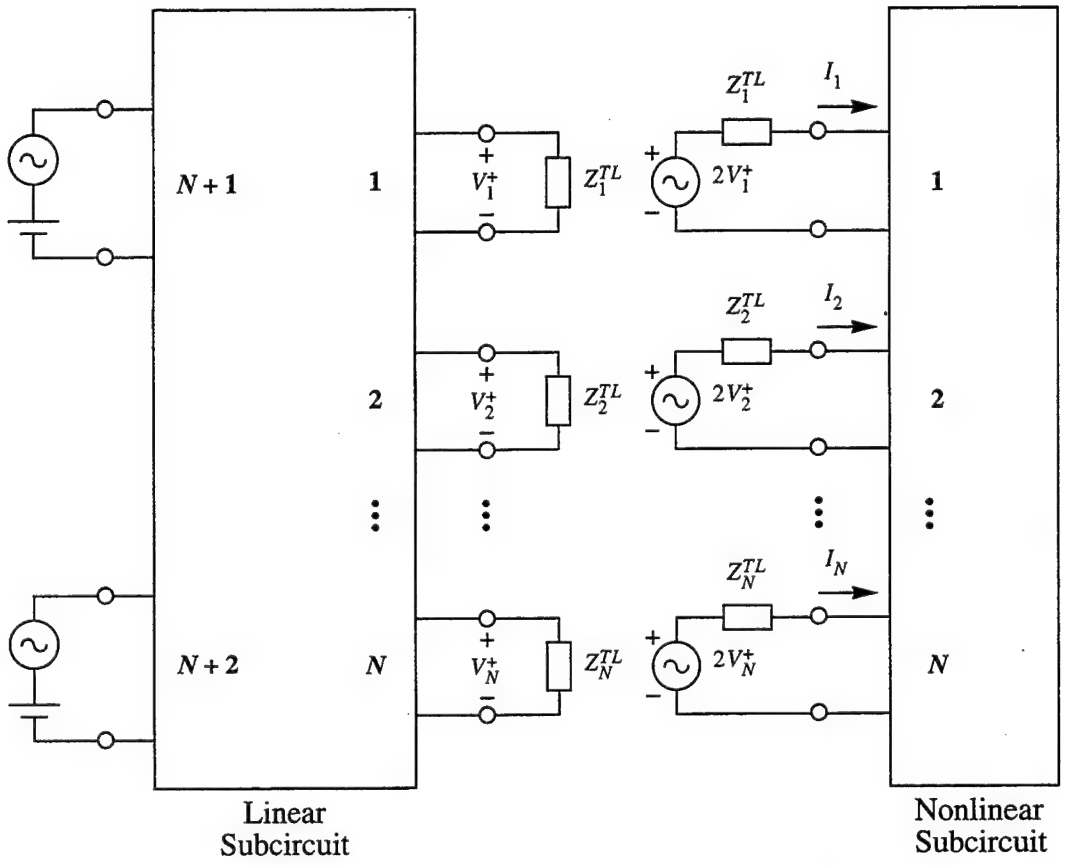

Figure 3.4 Incident wave circuit, equivalent to the circuit of Figure 3.3, used to determine the total harmonic voltage across the terminals of the intrinsic device.

can only be obtained by solving the resulting equivalent circuit of Figure 3.4 in the time-domain using an explicit time-discretization scheme. In order to maintain reasonable accuracies and avoid numerical instabilities, very small time steps are typically required. Since numerical device simulators employing implicit time-discretization schemes, such as those of Chapter 2, allow for much larger time steps, the MR algorithm cannot utilize the full efficiency of modern numerical device simulators. This problem is exacerbated whenever it is necessary to simulate several periods to achieve at least one "clean" steady-state cycle for Fourier analysis. When a device equivalent circuit or "power series" analytical model is used, the time integration of the nonlinear circuit differential equations can be a primary source of instability. As a result, high-order, step-controlled Runge-Kutta methods are typically employed. These methods are computationally expensive, however,

as they require numerous function evaluations for every time step taken. Overall, the availability of a harmonic-balance method that preserves the robust convergence properties of the MR algorithm, but impresses the total harmonic voltages directly across the terminals of the nonlinear device active region is highly desirable.

3.2 The Accelerated Fixed-Point Harmonic-Balance Circuit Analysis Technique

In order to utilize the full efficiency of the numerical device simulators of Chapter 2 and effectively integrate these simulators with a nonlinear circuit analysis technique, a fixed-point iterative harmonic-balance circuit analysis technique, derived from the robust multiple-reflection algorithm and termed the Accelerated Fixed-Point (AFP) harmonic-balance method[3.9], has been utilized. The AFP harmonic-balance method updates the total harmonic voltages applied directly across the active region of the device in terms of the impedances of the embedding circuit, the harmonic components of the current, and the harmonic components of the voltage from previous iterations. In equation form, the new voltage component at the intrinsic device terminals, for harmonic number n and iteration step k+1, is

$$V_{n,k+1} = \left(\frac{Z_n^{TL}}{Z_n^{Circuit} + Z_n^{TL}}\right) V_n^{Source} + \left(\frac{Z_n^{Circuit}}{Z_n^{Circuit} + Z_n^{TL}}\right)(V_{n,k} - I_{n,k} Z_n^{TL}) \tag{3.1}$$

where Z_n^{TL}, $Z_n^{Circuit}$, V_n^{Source}, and $I_{n,k}$ are the fictitious transmission line characteristic impedance, Thévenin equivalent impedance and source voltage of the linear embedding circuit at harmonic number n, and the device current component for harmonic number n and iteration step k, respectively. A detailed derivation of this equation is given in Appendix C. As shown in this appendix, the novelty in the AFP harmonic-balance algorithm lies in the use of *a priori* knowledge, from Kirchhoff's voltage law, that the nonlinear device impedance will equal the negative of the linear embedding impedance of the circuit for each of the undriven harmonics in the steady state. Again, it is important to note that this method updates the total harmonic voltages applied directly across the active region of the device. This eliminates the computationally expensive and possibly unstable Runge-Kutta

numerical time-integration which was required in the original multiple-reflection algorithm[3.10, 3.11] to obtain the harmonic voltages at the terminals of the intrinsic device.

Equation (3.1) can be rewritten, in a form similar to the voltage update method of references [3.12] and [3.13], as

$$V_{n,k+1} = d_n (V_n^{Source} - I_{n,k} Z_n^{Circuit}) + (1 - d_n) V_{n,k} \tag{3.2}$$

where

$$d_n = \frac{Z_n^{TL}}{Z_n^{Circuit} + Z_n^{TL}}. \tag{3.3}$$

Unlike the voltage update method, however, the AFP harmonic-balance algorithm utilizes complex under-relaxation parameters (d_n) for each harmonic component of the voltage waveform. These under-relaxation parameters provide varying degrees of damping for the harmonic voltage updates based on the relative magnitudes of the linear embedding impedances of the circuit, $Z_n^{Circuit}$, and enable the nonlinear mapping of equation (3.2) to produce a contracting (Cauchy) sequence with monotonic convergence properties[3.9].

A Steffenson numerical acceleration scheme for iterative equations, derived from the secant methods of numerical analysis[3.14, 3.15], is utilized for most simulations to greatly increase the computational speed and convergence properties of the AFP harmonic-balance circuit analysis method. The new voltage component at the intrinsic device terminals, for harmonic number n and iteration step k+1, then becomes

$$V_{n,k+1} = \tilde{V}_{n,k+2} + \frac{\left(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1}\right)\left(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1}\right)}{\left(\tilde{V}_{n,k+1} - V_{n,k}\right) - \left(\tilde{V}_{n,k+2} - \tilde{V}_{n,k+1}\right)} \tag{3.4}$$

where $\tilde{V}_{n,k+2}$ and $\tilde{V}_{n,k+1}$ are intermediate voltage values calculated from two successive applications of equation (3.1), starting with $\tilde{V}_{n,k} = V_{n,k}$. Overall, the AFP harmonic-balance circuit analysis technique outlined above avoids the laborious numerical

calculations needed in Newton-type techniques to assemble Jacobian matrices and solve large linear systems of equations, while maintaining a convergence rate nearly equal to that of Newton-type methods.

3.3 *Unified Numerical Device/AFP Harmonic-Balance Circuit Simulator for Frequency Multiplier Circuits*

Figure 3.5 shows a flow diagram of the algorithm utilized for numerical device/AFP harmonic-balance circuit simulations of frequency multiplier circuits. As illustrated in this diagram, the pump signal power level ($P_{available}$) and frequency, device d.c. bias ($V_{d.c.}$), embedding impedances of the circuit (d.c., and 1st through N^{th} harmonic), device material parameters including the alloy composition and doping profiles of the device active region and the resistivities of the ohmic contacts, device and chip dimensions, and device and circuit simulation convergence parameters are all adjustable inputs to the unified simulator. Outputs from the simulator include the steady-state current and voltage waveforms, intrinsic device impedances, circuit output powers (d.c., and 1st through N^{th} harmonic), and intrinsic device and circuit conversion efficiencies. In addition, device electric field, electron concentration, bandstructure, and particle, displacement, and total current profiles versus time and position can be obtained from the simulator.

The main portion of the unified simulation algorithm is as follows. The time-domain current through the device active region is calculated by the appropriate numerical device simulator, for one oscillation (pump) cycle, as described in Chapter 2. Due to initial simulation transients, two full periods are simulated during the first pass through the simulation algorithm such that the second "clean" period can be decomposed via Fourier analysis. For the device simulation, the total time-domain voltage across the terminals of the intrinsic device is found from the harmonic components of the voltage; initially, only the fundamental harmonic is present. The harmonic components of the current are extracted from the resulting time-domain current waveform using a discrete Fourier transform for periodic waveforms. The Fourier transform utilized in this work is based on the trigonometric Fourier series

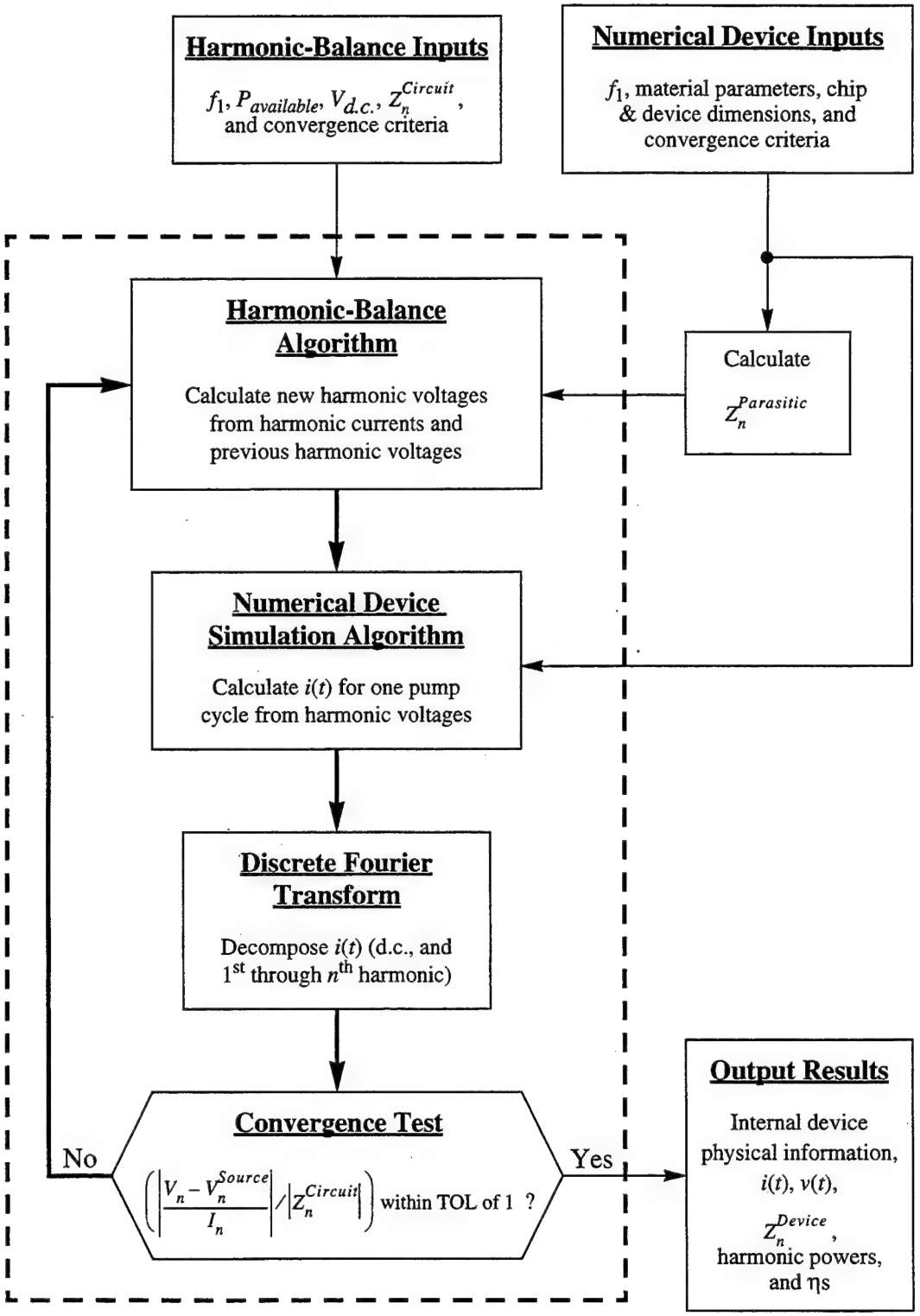

Figure 3.5 Unified numerical device/AFP harmonic-balance circuit simulation algorithm for frequency multipliers.

$$V(t) = \frac{1}{2}A_0 + \sum_{n=1}^{\infty} [A_n \cos(n\omega t) + B_n \sin(n\omega t)] \tag{3.5}$$

where the d.c. voltage is $\frac{1}{2}A_0$, the real part of a harmonic voltage is A_n, and the imaginary part of a harmonic voltage is $-B_n$. As a result, the magnitude of a harmonic voltage is

$$|V_n| = \sqrt{A_n^2 + B_n^2} \tag{3.6}$$

and the phase of a harmonic voltage is

$$\angle V_n = \text{atan}\left(\frac{-B_n}{A_n}\right). \tag{3.7}$$

The actual trigonometric Fourier transform is performed using the double precision IBM SSP routine DFORIT[3.11]. For SBVs, the discrete Fourier transform has been limited to six harmonics plus the d.c. term. Since the even harmonic components of the time-domain current waveform for an HBV are negligible, the discrete Fourier transform for HBVs has been extended to include thirteen harmonics plus the d.c. term.

Once the harmonic components of the total device current are extracted from the numerical device simulator time-domain current waveform, the AFP harmonic-balance circuit analysis scheme is used to update the total voltage applied directly across the active region of the device in terms of the impedances of the embedding circuit, the harmonic components of the current, and the harmonic components of the voltage from previous iterations. This iterative process is repeated until the harmonic components of the voltage converge to their steady-state values, or

$$\left|\frac{(V_n - V_n^{Source})}{I_n}\right| / \left|Z_n^{Circuit}\right| \tag{3.8}$$

is within a user-specified convergence factor of unity for all harmonics; this convergence factor is typically set to about 0.1 percent. On a Hewlett-Packard Apollo 9000 Series 735 workstation, the execution time of the unified simulator, in real (wall) time, is in the range

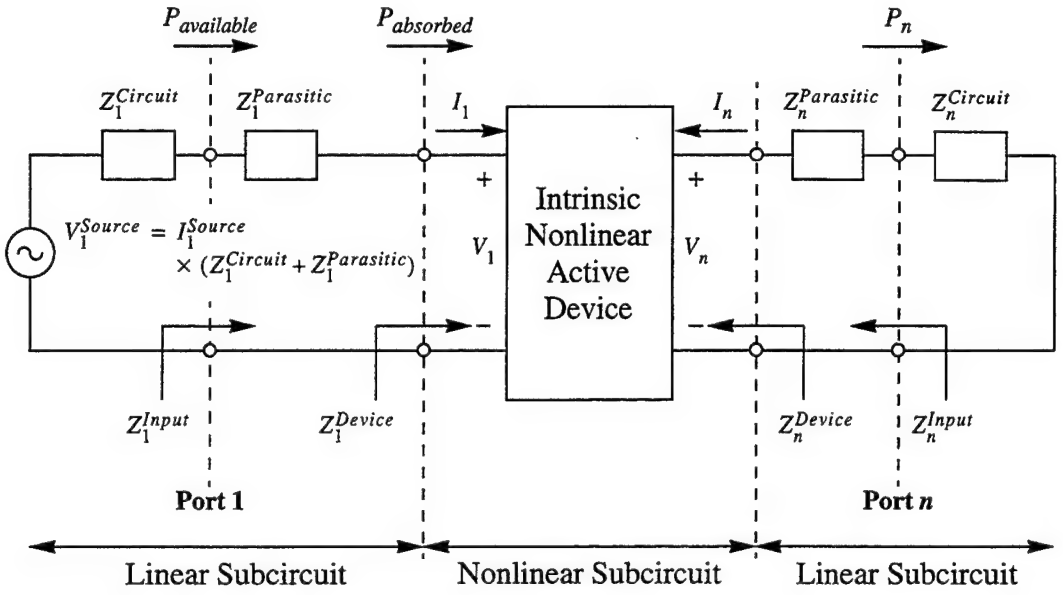

Figure 3.6 Schematic representation of a frequency multiplier circuit used for the calculation of multiplier port impedances and conversion properties.

of about one to seven hours for SBV structures, and in the range of about five to fifteen hours for HBV structures. These execution times are critically dependent on the number of mesh points utilized in the numerical device simulation, and on the impedances of the fictitious transmission lines, the convergence factor, and the embedding impedances of the circuit in the AFP harmonic-balance circuit analysis. For HBV structures, considerable reduction in simulation time may be possible by neglecting the even harmonic components in the voltage update scheme since the magnitudes of these components are negligible.

Frequency-dependent parasitic impedances, external to the active region of the device, are included in the harmonic-balance circuit analysis, at each of the harmonics of interest, as additional contributions to the linear device embedding circuit (see Figure 3.6). The d.c. parasitic impedance is used to calculate the actual device d.c. bias based on the d.c. current component found from the harmonic-balance circuit analysis. The parasitic device impedances are based on either a whisker-contacted or planar chip geometry, and are detailed in Appendix D. It is important to note that the parasitic impedances of interest here are those *external* to the active region of the nonlinear device. Although parasitics internal to the active region of the nonlinear device, such as the bias-dependent resistance and

shunting capacitance of the undepleted regions of the device[3.16], are detrimental to ideal device operation, these impedances are fully and self-consistently accounted for via the numerical device simulator.

Given the parasitic device impedances ($Z_n^{Parasitic}$), and the harmonic voltage (V_n) and harmonic current (I_n) components calculated from the harmonic-balance circuit analysis, a frequency multiplier's port (harmonic) impedances and conversion properties can be calculated based on the circuit of Figure 3.6. The input impedance of the multiplier at any port n is

$$Z_n^{Input} = Z_n^{Parasitic} + \frac{V_n}{I_n} \tag{3.9}$$

where the second term on the right-hand side of this equation is the impedance of the intrinsic device at harmonic n (Z_n^{Device}). The power available from the pump at the multiplier input port (port 1) is

$$P_{available} = \frac{|V_1^{Source}|^2}{8Re\{Z_1^{Circuit}\}}. \tag{3.10}$$

Since $P_{available}$ is an input to the simulator, the pump voltage, V_1^{Source}, is calculated from equation (3.10) for use in the harmonic-balance algorithm outlined above. Due to impedance mismatch at the input to the multiplier, only a portion of the available pump power is typically absorbed by the intrinsic device; the portion of the available pump power absorbed by the intrinsic device is

$$P_{absorbed} = \frac{1}{2}Re\{Z_1^{Device} + Z_1^{Parasitic}\}|I_1|^2, \quad n>1. \tag{3.11}$$

The power delivered to port n with impedance $Z_n^{Circuit}$ is

$$P_n = \frac{1}{2}Re\{-Z_n^{Device} - Z_n^{Parasitic}\}|I_n|^2 = \frac{1}{2}Re\{Z_n^{Circuit}\}|I_n|^2. \tag{3.12}$$

Since there is typically only one output port, and only a portion of the absorbed power is converted to the characteristic frequency of this port, the power dissipated in the multiplier device is the difference between the absorbed power and the power delivered to the output port (P_{output}). Finally, the conversion efficiency of the *intrinsic* frequency multiplier is

$$\eta_{Intrinsic} = \frac{P_{output}}{P_{absorbed}} \tag{3.13}$$

while the multiplier *circuit* conversion efficiency is

$$\eta_{Circuit} = \frac{P_{output}}{P_{available}}. \tag{3.14}$$

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Chapter 4

Thermal Analysis of Whisker-Contacted and Planar Geometry Frequency Multipliers

In addition to investigating the electrical characteristics of Heterostructure Barrier Varactor (HBV) and Schottky Barrier Varactor (SBV) frequency multiplier circuits, the thermal properties of these circuits must also be analyzed due to the large amount of power that can be dissipated in the varactor device itself. The thermal analysis presented in this chapter is a steady-state analysis based on the amount of power dissipated in the active region of the device and the thermal resistance to heat flow presented by the various elements that make up the circuit in which the device is embedded. From these quantities, the average temperature across the active region of the varactor device can be estimated for use in the appropriate numerical device simulator. Although the present focus is on HBV frequency multiplier circuits, the analysis approach presented here can be applied to a wide range of solid-state devices and circuits; only minor modifications to the thermal resistance equivalent circuits and thermal resistance expressions given here are required to analyze the thermal properties of SBV frequency multiplier circuits.

4.1 Thermal Resistances of Frequency Multiplier Circuit Constituent Elements

The thermal model presented here uses simple geometrical expressions for the thermal resistances of the various elements that make up circuits having both whisker-contacted and planar device geometries. For planar devices, however, the substrate thermal resistance is not amenable to description by simple geometrical expressions. As such, it is calculated numerically using a three-dimensional finite-element heat flow analysis program[4.1]. For all elements surrounded by air, it is assumed that the ambient air is a perfect thermal insulator.

4.1.1 *Thermal Resistances of General Circuit Elements*

For heat flow through a bulk section of material which is surrounded by air (see Figure 4.1a), the thermal resistance is

$$R_{Thermal} = \frac{t}{\kappa \pi r^2} \tag{4.1}$$

where t is the thickness of the section, r is an equivalent radius based on the cross-sectional area of the section, and κ is the material's thermal conductivity. Likewise, for heat flow through a heat contact and into a multilayer stack of materials which is surrounded by air (see Figure 4.1b), the approximate thermal resistance of the first layer is[4.2, 4.3]

$$R_{Thermal} = \frac{t}{\kappa_1 \pi \left(\frac{1}{2}(r_1 + r_2)\right)^2} \tag{4.2}$$

where r_1 is an equivalent radius based on the cross-sectional area of the heat contact through which heat flows into the multilayer stack, and

$$r_2 = r_1 + t\tan\theta\,. \tag{4.3}$$

Following reference [4.2], the heat flux is assumed to be transmitted within a truncated right circular cone of vertex angle θ. A vertex angle of 45° is used here as this angle yields results which closely approximate more exact computer simulations of the heat flow[4.2]. For heat flow into a semi-infinite heat sink (see Figure 4.1c), the thermal resistance is given by

$$R_{Thermal} = \frac{1}{4\kappa r} \tag{4.4}$$

where, again, r is an equivalent radius based on the cross-sectional area of the heat contact through which heat flows into the heat sink.

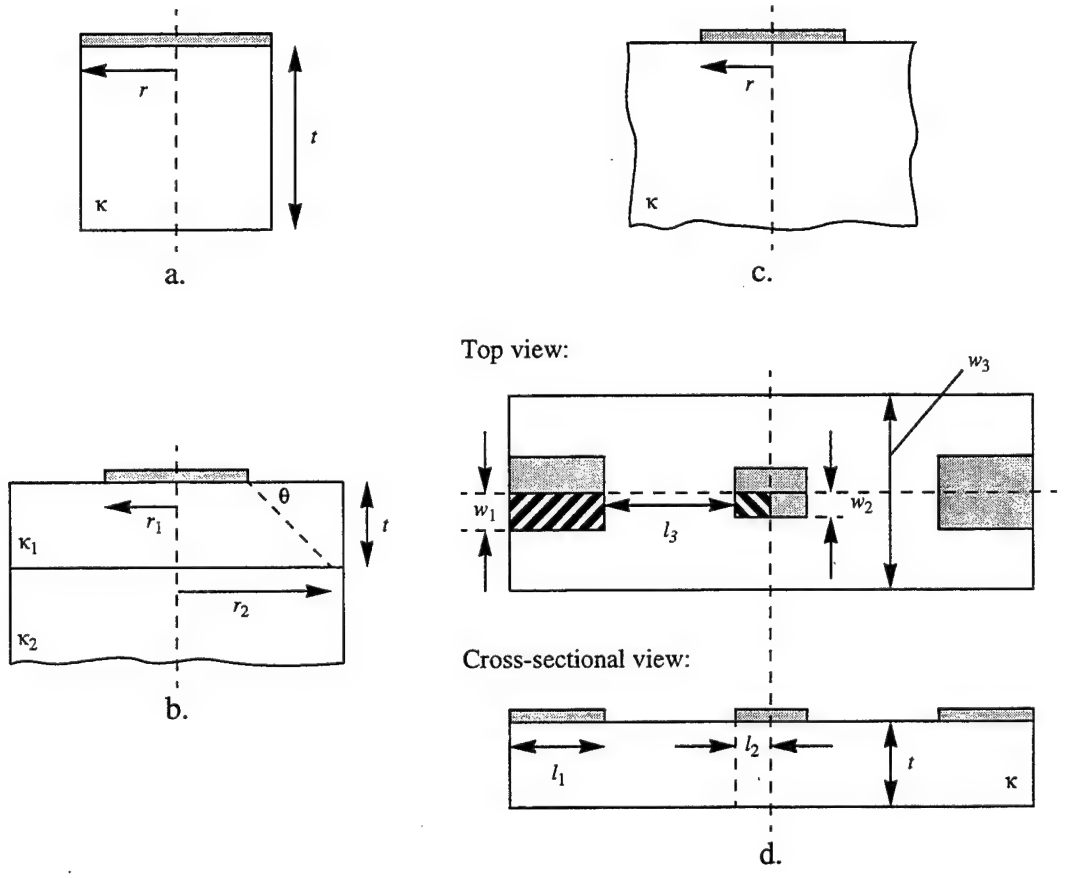

Figure 4.1 Relevant geometries for the constituent elements of a multiplier circuit: (a.) bulk section of material surrounded by air, (b.) multilayer stack of materials, (c.) semi-infinite heat sink, and (d.) planar device pair substrate configuration (top and cross-sectional views) with input (w_1 x l_1) and output (w_2 x l_2) heat flow "ports"[4.4].

4.1.2 Thermal Resistance of the Planar Geometry Device Substrate

For planar devices, the thermal resistance of the device substrate is calculated using a three-dimensional finite-element heat flow analysis program[4.1] to account for the substrate's irregular heat flow geometry. Due to symmetry considerations, only a quarter of the actual planar substrate is simulated. The heat flow analysis program is utilized to calculate the amount of power required to generate a 1 K temperature gradient between the input and output heat flow "ports" of the substrate assuming a uniform heat flux into and out of the substrate, a constant substrate thermal conductivity, and perfectly insulating substrate boundaries. With this information, the substrate thermal resistance (K/W) is

simply 1 K divided by the amount of power required to realize this temperature gradient. The finite element mesh utilized for the present calculations consisted of square blocks with sides 5 μm in length. The planar geometry considered here (see Figure 4.1d) is that of a planar device pair, with dimensions that correspond to the δ-doped anti-series SBV of reference [4.4]. This geometry is of particular interest as it is the geometry utilized for the planar HBVs described in Chapter 6.

Figure 4.2 shows the calculated planar substrate thermal resistance as a function of substrate thickness t and input heat flow "port" width w_2. The important result to note from this figure is that, to achieve optimum heat sinking with a GaAs substrate and the typical device dimensions shown, the substrate should not be thinned below about 2 mils. As such, all subsequent calculations assume a substrate thickness of 3 mils. Since the length of the air bridge "finger" is often varied to control the parasitic pad-to-pad capacitance of a planar device, it is important to examine the substrate thermal resistance as a function of the "finger" length. For the present calculations, the "finger" length is varied by changing the separation between the input and output heat flow "ports." Since the output heat flow "port" comprises only half of the contact pad, the actual "finger" length is $l_3 - l_1$. Figure 4.3 shows the calculated planar substrate thermal resistance as a function of "finger" length $l_3 - l_1$ and input heat flow "port" width w_2. From this figure, it is clear that the substrate thermal resistance scales linearly with the "finger" length, but is not a strong function of this length. Finally, the calculated planar substrate thermal resistance, as a function of substrate thermal conductivity and input heat flow "port" width w_2, is shown in Figure 4.4 along with analytical fits to the calculated resistances; nominal values of 3 mils and 42 μm for the substrate thickness and "finger" length, respectively, have been used in these calculations.

4.2 Calculation of the Average Active Region Temperature in a Frequency Multiplier

With a known amount of power dissipated in the active region of a multiplier device (for example, from the harmonic-balance circuit analysis of Chapter 3), the steady-state linear temperature gradient across each element of the multiplier circuit is simply the product of the power flowing through the particular element and the thermal resistance of

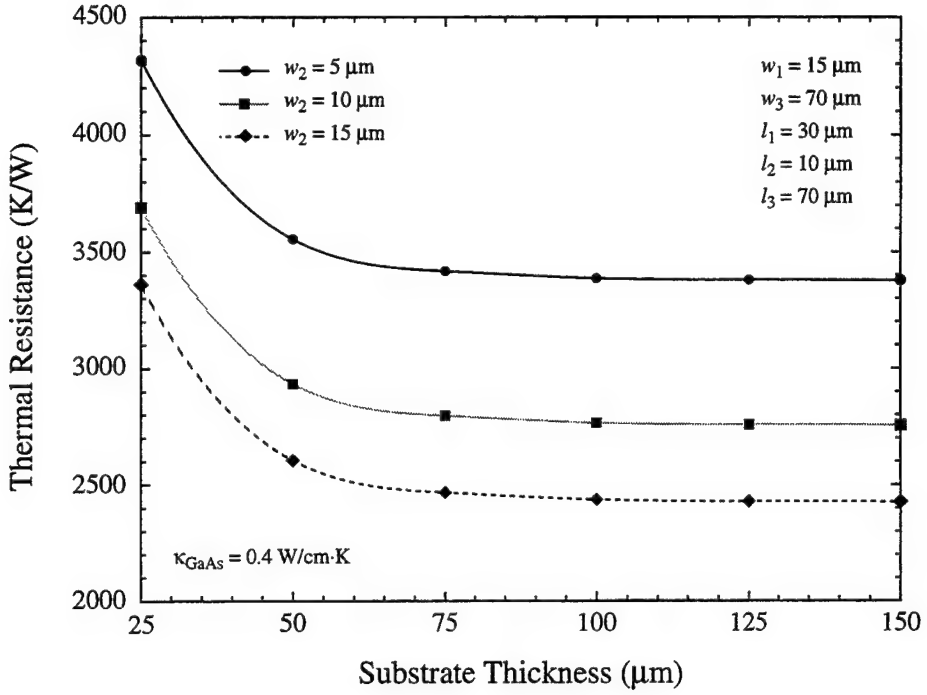

Figure 4.2 Substrate thermal resistance versus substrate thickness t and input heat flow "port" width w_2 for half of a planar device pair.

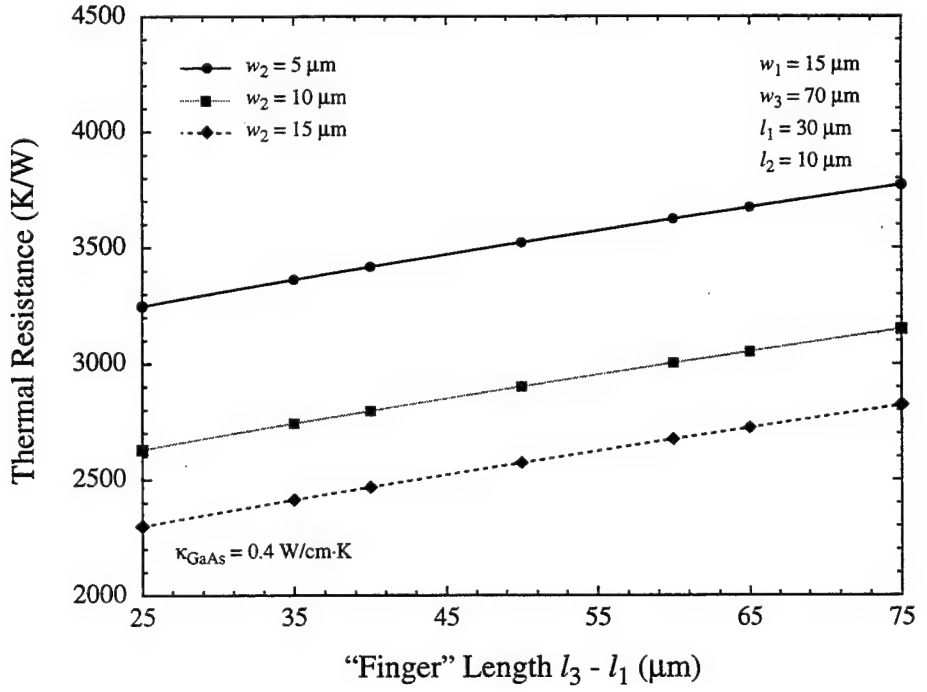

Figure 4.3 Substrate thermal resistance versus "finger" length l_3 - l_1 and input heat flow "port" width w_2 for half of a planar device pair.

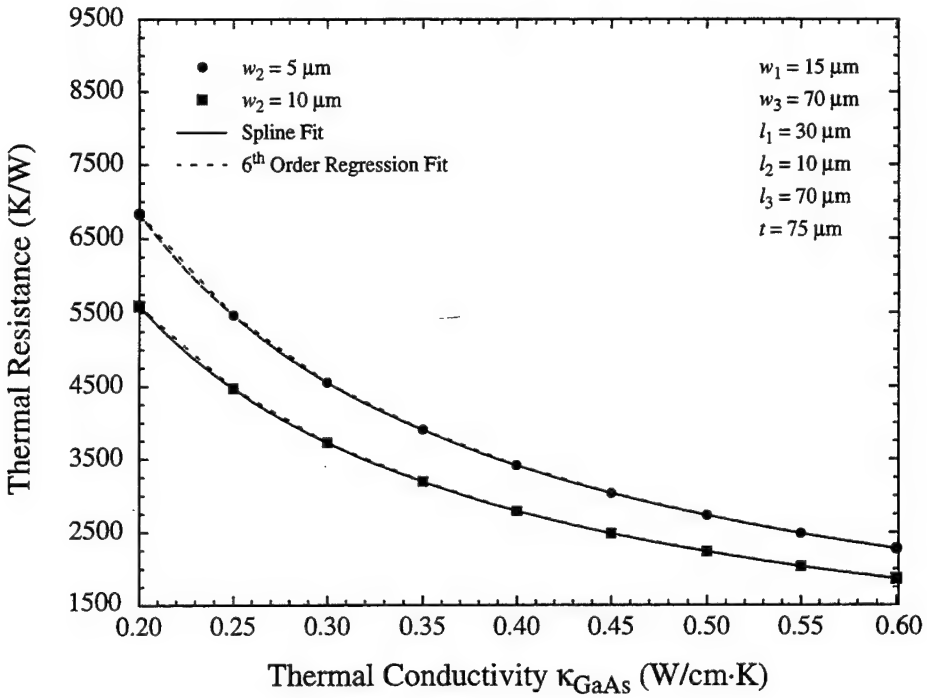

Figure 4.4 Substrate thermal resistance versus substrate thermal conductivity and input heat flow "port" width w_2 for half of a planar device pair.

the element. From this information, the average temperature across the active region of the varactor device can be estimated for use in the appropriate numerical device simulator. For simplicity, it is assumed that all of the dissipated power is absorbed in the center of the device active region.

4.2.1 Thermal Resistance Equivalent Circuits for HBV Whisker-Contacted and Planar Geometry Frequency Multipliers

Representative HBV whisker-contacted and planar multiplier circuits are shown in Figures 4.5 and 4.6, respectively. Since these circuits have more than one heat flow path to reach equilibrium with the ambient air, an equivalent circuit representation of the actual circuit's thermal resistances is used to calculate the portion of the total dissipated power that flows through each path of the equivalent circuit. For example, in the planar device pair configuration, there are two parallel heat flow paths (parallel heat flow, through the "finger" and through the substrate, to the contact pad) for each device in the configuration. The thermal resistance equivalent circuits for the representative HBV multiplier circuits of

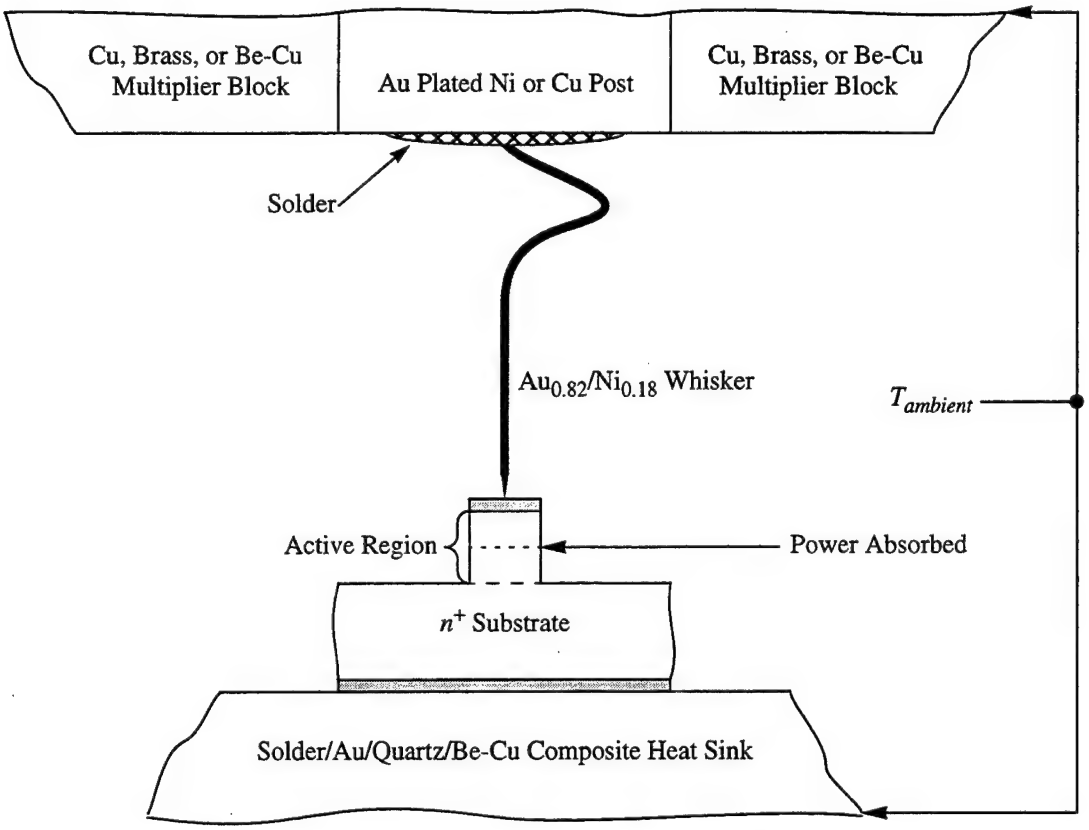

Figure 4.5 Representative whisker-contacted geometry HBV multiplier circuit. Circuit temperature is assumed to reach equilibrium with the ambient air at the locations indicated. The dissipated power is assumed to be absorbed in the center of the device active region as shown.

Figures 4.5 and 4.6 are shown in Figures 4.7 and 4.8, respectively. Explicit equations are given in Appendix E for the various thermal resistances that make up these equivalent circuits.

It is important to note that the thermal resistances for all of the constituent elements that make up these equivalent circuits, with the exception of the composite heat sink in Figures 4.5 and 4.6 and the substrate in Figure 4.6, can be strictly described by equations (4.1), (4.2), and (4.4). The composite heat sink of Figures 4.5 and 4.6 encompasses the heat sinking properties of the typical low-pass microstrip filter circuit (Au on quartz) which is bonded to the Be-Cu multiplier block and to which the multiplier device is soldered. Although this heat sink has an extremely complex geometry and material

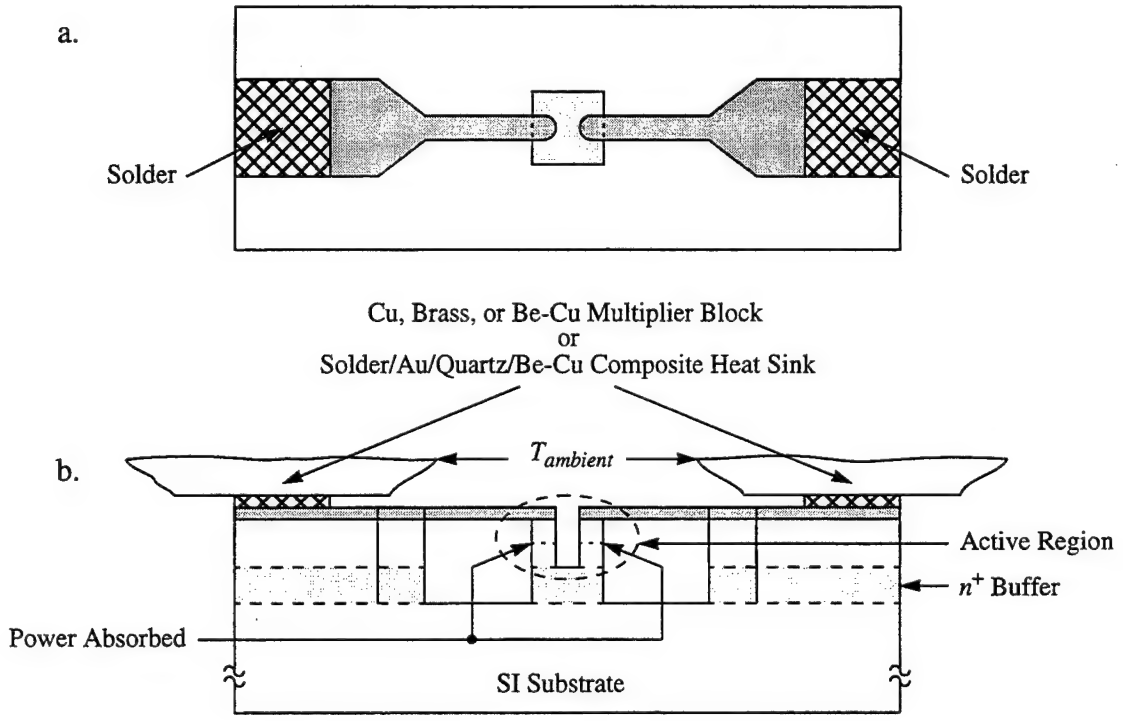

Figure 4.6 Top (a.) and cross-sectional (b.) views of a representative planar geometry HBV multiplier circuit. Circuit temperature is assumed to reach equilibrium with the ambient air at the locations indicated. The dissipated power is assumed to be absorbed in the center of the device active region as shown.

composition, it is modeled simply as a semi-infinite heat sink to facilitate the present analysis.

4.2.2 Temperature-Dependent Thermal Conductivities for HBV Frequency Multiplier Circuit Materials

To further simplify the analysis, the thermal conductivity of each element in the circuit is taken to be a constant value, as a function of position, that is determined by the average temperature across the element. The thermal conductivities of the metallic portions of Figures 4.5 and 4.6 vary slowly with temperature between 200 K and 500 K, and are therefore assumed equal to their values at 300 K (κ_{Au} = 3.17 W/cm·K[4.5], κ_{Ni} = 0.907 W/cm·K[4.5], κ_{Cu} = 4.01 W/cm·K[4.5], and $\kappa_{Brass/Be\text{-}Cu} \approx$ 1.0 W/cm·K[4.5]). A nominal temperature-independent thermal conductivity of 0.5 W/cm·K is used for the composite heat sink of Figures 4.5 and 4.6. The semiconductor portions of

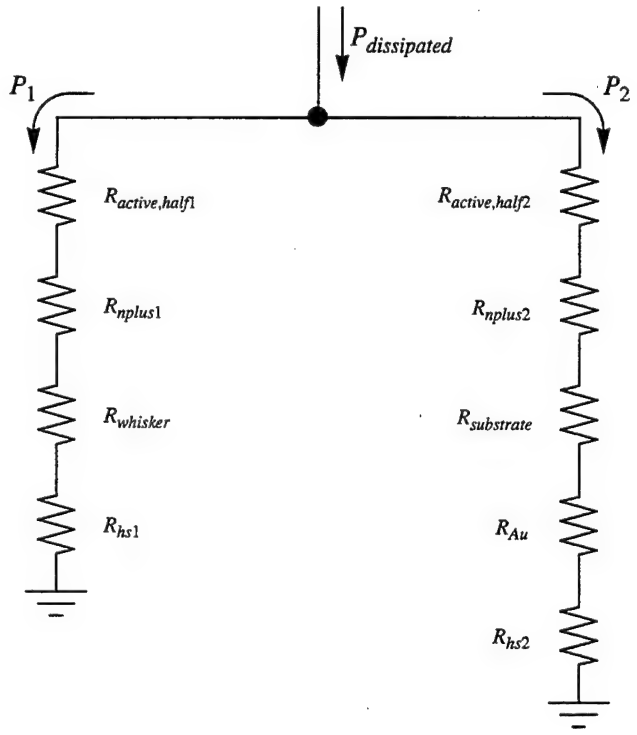

Figure 4.7 Thermal resistance equivalent circuit for the representative whisker-contacted geometry HBV multiplier circuit of Figure 4.5.

Figures 4.5 and 4.6 have the largest variation in thermal conductivity with temperature. For GaAs, which constitutes the majority of the semiconductor material being considered, the thermal conductivity follows a

$$\kappa_{GaAs} = \frac{A}{T^{1.2}} \tag{4.5}$$

law[4.6] where A varies with doping level. For GaAs doped at $N_D = 1x10^{17}$ cm^{-3}, $A = 488$ while $A = 366.5$ for highly doped GaAs and $A = 544$ for lightly doped GaAs[4.6]. Although the active region mesas of actual devices to be considered contain $In_xGa_{1-x}As$ and $Al_xGa_{1-x}As$ layers, these layers are assumed to have thermal conductivities equivalent to those of the active region GaAs layers to simplify the analysis. This assumption is valid since the $In_xGa_{1-x}As$ and $Al_xGa_{1-x}As$ layers are extremely thin and their actual thermal conductivities are comparable to that of GaAs[4.7, 4.8].

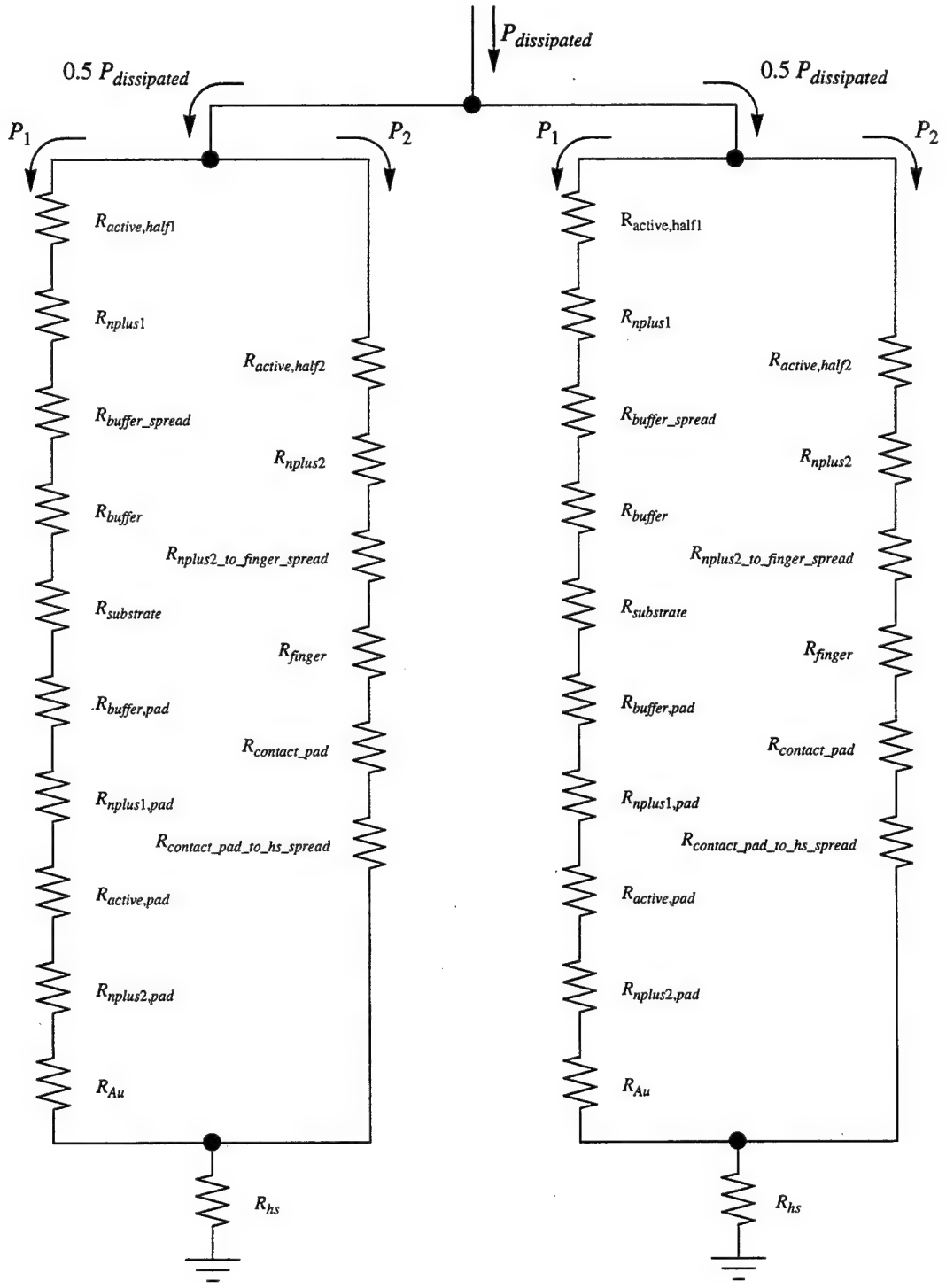

Figure 4.8 Thermal resistance equivalent circuit for the representative planar geometry HBV multiplier circuit of Figure 4.6.

Since the thermal conductivity of each element is allowed to vary with the average temperature across the element, the process outlined at the beginning of *Section 4.2* is an iterative one. For this work, convergence was achieved when the temperature change, from one iteration to the next and across all of the circuit elements, was less than 0.1 K.

4.3 Comparison of Whisker-Contacted and Planar Geometry HBV Frequency Multiplier Thermal Properties

Using the thermal analysis presented in the preceding sections, the thermal properties of two HBV frequency multiplier circuits have been examined, one using a whisker-contacted geometry device (see Figure 4.5) and a companion one using a planar geometry device (see Figure 4.6). Although the results presented here are for HBVs, it is important to reiterate that the conclusions drawn from these results apply to both HBVs and SBVs since the thermal analysis is based on geometry rather than device properties. SBVs can be analyzed using the same general thermal analysis procedure outlined in the preceding sections. The thermal resistance equivalent circuits and the expressions for the constituent thermal resistances would require minor modifications, however, to account for the slight differences in geometry and device structure between the HBV and the SBV.

Both HBV frequency multiplier circuits utilized devices having GaAs/$Al_xGa_{1-x}As$ epitaxial structures, 8 μm diameter anodes and 3 mil thick substrates. A 1.4 μm thick double barrier epitaxial structure was used for the planar geometry device, yielding a four barrier device due to the back-to-back configuration of this geometry; for the whisker-contacted geometry device, a 2.8 μm four barrier epitaxial structure was used. The whisker-contacted geometry device had an n^+ GaAs substrate (A = 366.5) while the planar geometry device had a semi-insulating (SI) GaAs substrate (A = 544). The whisker-contacted multiplier circuit utilized a 0.2125 mm long[4.9], 1 mil diameter $Au_{0.82}/Ni_{0.18}$ whisker. Critical dimensions for the planar geometry device are as follows: n^+ GaAs buffer 4 μm thick, diced chip 220 μm long and 70 μm wide, Au metallized "fingers" 2.5 μm thick, 42 μm long, and 8 μm wide, Au metallized bonding pads 2.5 μm thick, 60 μm long, and 30 μm wide, and anodes separated by 5 μm. The output heat flow "port" was assumed to

comprise only half of the bonding pad length and, thus, was assumed to be 30 μm long and 30 μm wide.

Figure 4.9 shows the calculated average active region temperature for these two multiplier circuits assuming an ambient temperature of 300 K. For whisker-contacted geometry HBV frequency multipliers, the elements in the two heat flow paths with the largest thermal resistance to heat flow are the substrate ($R_{substrate}$) and the whisker ($R_{whisker}$). With the typical whisker-contacted device dimensions given above and 50 mW of dissipated power, the substrate thermal resistance was 254.4 K/W while the whisker thermal resistance was 465.6 K/W. A reduction in the substrate thickness or the whisker length would lead to a proportional reduction in the substrate or whisker thermal resistances. Likewise, for planar geometry HBV frequency multipliers, the elements in the two heat flow paths (half of the planar device pair) with the largest thermal resistance to heat flow are the substrate ($R_{substrate}$) and the "finger" (R_{finger}). With the typical planar device dimensions given above and 50 mW of dissipated power, the substrate thermal resistance was 903.6 K/W while the "finger" thermal resistance was 1332.4 K/W. Both the substrate and "finger" thermal resistances can be reduced by shortening the length of the "finger".

Although the dominant thermal resistances in these circuits can be reduced by appropriately modifying the geometry of the multiplier device, it is important to note that the active device dimensions are influenced by both the electromagnetic and thermal properties of the device geometry. For example, the whisker length is determined primarily by the whisker inductance required to resonate the average capacitance of the device active region at a desired harmonic of the pump frequency; thermal considerations are secondary in determining the whisker length. For planar geometry multiplier devices, the length of the "finger" is determined by the allowable parasitic pad-to-pad capacitance and, to a much lesser extent, by the realizable inductance of the "finger". In this case, thermal considerations can play a much greater role in determining the device geometry since the electromagnetic considerations are not as critical as they are for whisker-contacted geometry multiplier circuits.

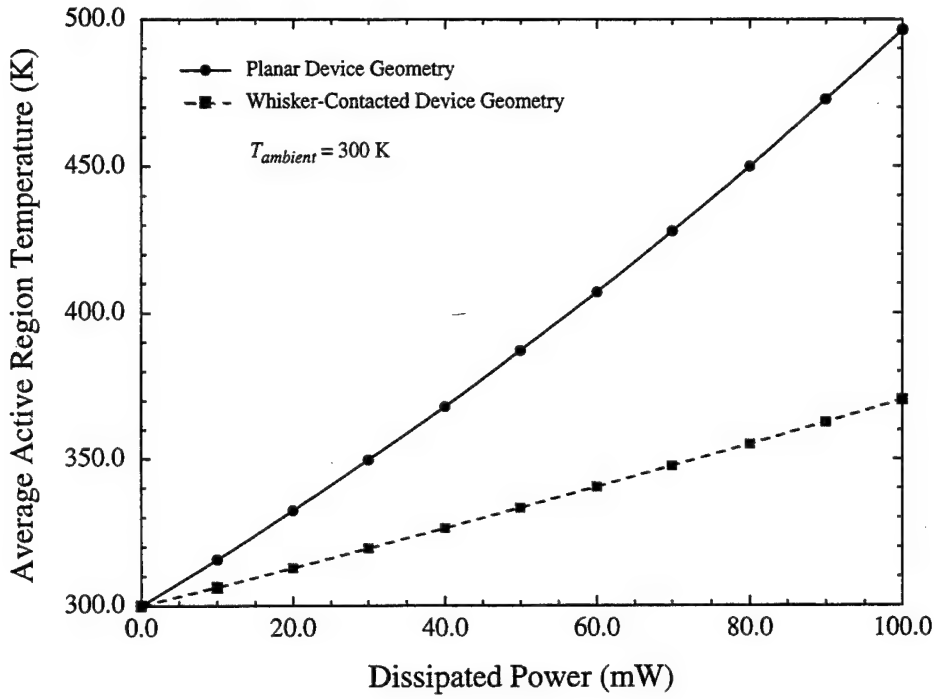

Figure 4.9 Average active region temperature versus power dissipated in the active region for the whisker-contacted and planar HBV device geometries of Figures 4.5 and 4.6.

With these concerns in mind, the design of any frequency multiplier circuit certainly requires trade-offs between the electromagnetic and thermal properties of the multiplier device. One such trade-off involves the choice of substrate material for planar geometry multiplier circuits[4.10]. From an electromagnetic point of view, the use of a low dielectric substrate such as quartz is desirable as it would reduce dielectric circuit losses. From a thermal point of view, however, the use of a quartz substrate in place of a GaAs substrate is not desirable since fused silica quartz has a thermal conductivity of only about 0.014 W/cm·K at 273 K and 0.016 W/cm·K at 373 K[4.5]. Although crystalline quartz has a slightly higher thermal conductivity of 0.12 W/cm·K and 0.068 W/cm·K at 273 K for its parallel and perpendicular orientations, these values are expected to decrease at temperatures above 273 K[4.5]. Hence, the replacement of the GaAs substrate with a quartz substrate would clearly exacerbate the problem of elevated average active region temperatures for planar geometry multiplier circuits (see Figure 4.9). Further study is required to fully examine the trade-off between the reduced dielectric circuit loss and the

increased average active region temperature of planar geometry multiplier circuits utilizing quartz substrates.

Overall, the comparisons of the thermal properties of whisker-contacted and planar geometry multiplier circuits presented in this chapter indicate that the average active region temperature in planar geometry devices can be significantly higher than the temperature in whisker-contacted geometry devices. Such elevated temperatures translate directly into lower carrier mobilities in the device active region and, consequently, to lower circuit multiplying efficiencies. As a result, careful consideration needs to be given to both thermal and electromagnetic properties when designing frequency multiplier circuits.

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[4.9] D. Choudhury, M. A. Frerking, and P. D. Batelaan, "A 200 GHz Tripler Using a Single Barrier Varactor," *IEEE Trans. Microwave Theory Tech.*, Vol. 41, No. 4, April 1993, pp. 595-599.

[4.10] J. Tuovinen and N. R. Erickson, "Finite Element Analysis of a Planar Diode Doubler," *Proc. Fourth Int. Symp. Space Terahertz Technol.*, March 30-April 1, 1993, Los Angeles, California, pp. 326-339.

Chapter 5

D.C., Large-Signal Sinusoidal, and Harmonic-Balance Simulation Results

In order to demonstrate the validity of the Heterostructure Barrier Varactor (HBV) numerical device simulator, comparisons have been made between d.c. device simulation results and published experimental d.c. current-voltage (I-V) and static capacitance-voltage (C-V) results for several HBV device structures. Large-signal time-dependent numerical device simulations of both HBV and Schottky Barrier Varactor (SBV) devices, assuming an ideal sinusoidal pump signal, have been compared to results obtained from standard HBV and SBV quasi-static equivalent circuit device models. These comparisons document the frequencies and drive levels at which the lumped quasi-static models diverge from the numerical device models on which they are based. More importantly, the large-signal sinusoidal comparisons elucidate the physical phenomena underlying the divergence of results for the two device modeling approaches. Finally, comparisons have been made between harmonic-balance circuit simulation results and published experimental frequency multiplication results for HBV frequency triplers and SBV frequency doublers. Again, the harmonic-balance results utilized both quasi-static equivalent circuit and numerical device models. These results accentuate the importance of using a numerical device model in place of the standard quasi-static equivalent circuit device model at high frequencies and drive levels, that is when phenomenon such as current saturation and electron velocity saturation dominate device operation.

5.1 Comparison of D.C. Device Simulation Results With Experimental D.C. I-V and Static C-V Results

The experimental d.c. I-V characteristics of several single barrier, 100 μm diameter, circular GaAs/$Al_{0.7}Ga_{0.3}As$ HBV devices (UVA-NRL-1172-E) fabricated at the University of Virginia (UVA) are shown in Figure 5.1 along with the simulated d.c. I-V curve. Details of the mesa-isolation fabrication process for these devices will be presented

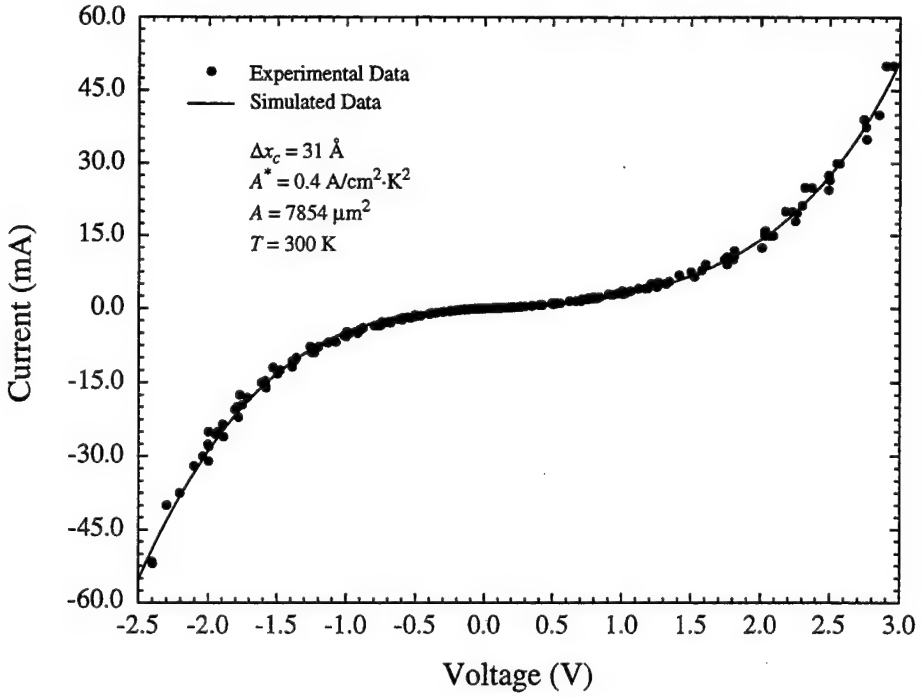

Figure 5.1 Experimental and theoretical d.c. I-V characteristics for the UVA-NRL-1172-E 100 μm diameter, circular mesa-isolated single barrier *n* GaAs/ *i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBVs.

in Chapter 6. As illustrated by this figure, excellent correlation between the numerical device simulator and the experimental d.c. I-V results for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBVs has been obtained. Figure 5.2 shows the simulated conduction-band structure of this device at a d.c. bias of 0.5 V. Discontinuities in the electron quasi-Fermi potential across the heterointerfaces, as dictated by equations (2.7) and (2.11), are clearly evident in this figure. For all simulations, unintentionally doped (undoped) layers were modeled as ideally intrinsic. In addition to the transport parameters shown in Figure 5.1, a drifted-Maxwellian electron effective mass ratio ($m^*_{D\text{-}M}/m_0$) of 0.6115 was used in the simulations. The current prefactor utilized here agrees with the results of Solomon *et al.*[5.1] for $Al_{0.7}Ga_{0.3}As$ barriers. The simulated device consisted of a 200 Å undoped $Al_{0.7}Ga_{0.3}As$ barrier surrounded by 50 Å undoped GaAs spacer layers and *n*-type GaAs modulation layers. The asymmetry in the d.c. I-V characteristics is attributed to asymmetry in the doping profile and modulation layer thicknesses as indicated by Secondary Ion Mass Spectroscopy (SIMS) analysis[5.2]. One modulation layer was shown to have a length of

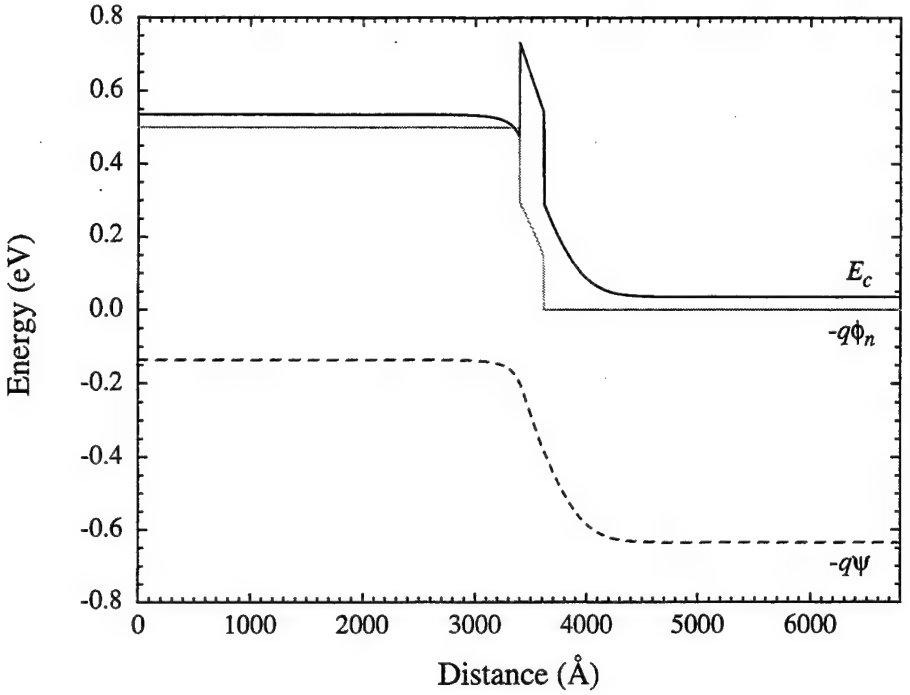

Figure 5.2 Calculated conduction-band structure of a single barrier *n* GaAs/ *i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV at a d.c. bias of 0.5 V.

about 1750 Å and a doping of approximately $9.5x10^{16}$ cm^{-3}, while the other modulation layer was about 2000 Å in length and was doped approximately $6.0x10^{16}$ cm^{-3}. The alloy composition of the 200 Å undoped AlGaAs barrier was also verified by SIMS to be 70% aluminum. Figure 5.3 shows the doping concentration and alloy composition profiles of this HBV structure as determined by the SIMS analysis.

Excellent correlation between the numerical device simulator and experimental d.c. I-V and static C-V data from the literature has also been obtained for single barrier $GaAs/Al_{0.7}Ga_{0.3}As$, $GaAs/Al_{0.4}Ga_{0.6}As$, and $GaAs/In_{0.2}Ga_{0.8}As/Al_{0.4}Ga_{0.6}As$ HBVs. For these comparisons, the simulated C-V characteristics were estimated from the state variables by calculating the change in charge with respect to the change in applied d.c. bias over the depletion side (barrier layer and depleted modulation layer) of the device for sufficiently small increments in the applied bias. Figure 5.4 shows excellent correlation between the simulated and experimental d.c. I-V and static C-V characteristics for the single barrier, 101.6 μm long, square $GaAs/Al_{0.7}Ga_{0.3}As$ HBVs of Hjelmgren *et al.*[5.3]. The simulated device consisted of a 215 Å undoped $Al_{0.7}Ga_{0.3}As$ barrier surrounded by

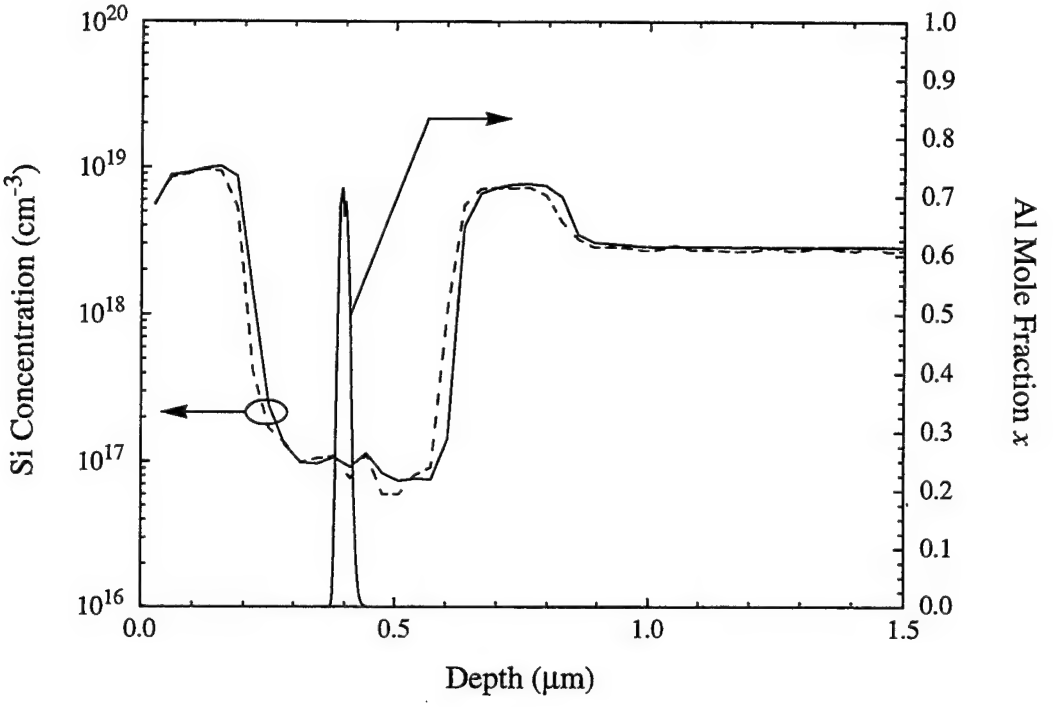

Figure 5.3 Si dopant concentration and barrier Al composition profiles, as determined by SIMS analysis, for the single barrier *n* GaAs/ *i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV (UVA-NRL-1172-E) of Figure 5.1.

55 Å undoped GaAs spacer layers and 3350 Å *n*-type ($1x10^{17}$ cm^{-3}) GaAs modulation layers. The drifted-Maxwellian electron effective mass ratio utilized for these simulations was the same as those used to simulate the UVA devices. In addition, the current prefactor required to reproduce the Hjelmgren *et al.* data matches the value required to reproduce data from the UVA devices, and agrees with the Solomon *et al.*[5.1] results for $Al_{0.7}Ga_{0.3}As$ barriers.

A final comparison of the numerical device simulator with experimental data is facilitated by the d.c. I-V and static C-V results of Krishnamurthi *et al.*[5.4, 5.5] for single barrier, 120 μm diameter, circular $GaAs/Al_{0.4}Ga_{0.6}As$ and $GaAs/In_{0.2}Ga_{0.8}As/Al_{0.4}Ga_{0.6}As$ HBVs. Figures 5.5 and 5.6 show excellent correlation between the simulated and experimental d.c. I-V characteristics for the $GaAs/Al_{0.4}Ga_{0.6}As$ and $GaAs/In_{0.2}Ga_{0.8}As/Al_{0.4}Ga_{0.6}As$ devices, respectively. Likewise, Figure 5.7 shows excellent correlation between the simulated and experimental static C-V characteristics for the $GaAs/In_{0.2}Ga_{0.8}As/Al_{0.4}Ga_{0.6}As$ devices. The simulated devices consisted of undoped

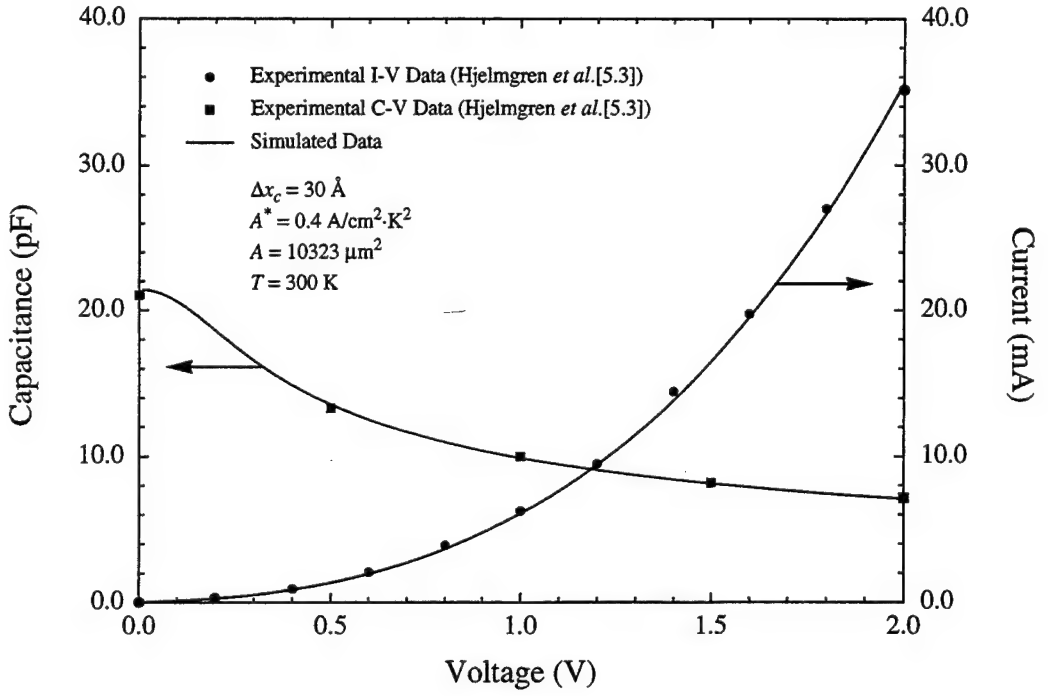

Figure 5.4 Experimental and theoretical d.c. I-V and static C-V characteristics for the 101.5 µm long, square mesa-isolated single barrier *n* GaAs/ *i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBVs of reference [5.3].

$Al_{0.4}Ga_{0.6}As$ barriers surrounded by undoped spacer layers and 3350 Å *n*-type GaAs modulation layers. The simulated GaAs/$Al_{0.4}Ga_{0.6}As$ device had 50 Å GaAs spacer layers and a 260 Å barrier while the simulated GaAs/$In_{0.2}Ga_{0.8}As$/$Al_{0.4}Ga_{0.6}As$ device had 60 Å pseudomorphic $In_{0.2}Ga_{0.8}As$ spacer layers and a 275 Å barrier. The asymmetry in the experimental d.c. I-V characteristics is attributed to asymmetry in the modulation layer doping profiles as indicated by SIMS analysis[5.5]. The estimated modulation layer doping profiles were graded from $1.1x10^{17}$ cm^{-3} to $9.0x10^{16}$ cm^{-3} on the cathode side of the barrier and from $7.0x10^{16}$ cm^{-3} to $5.0x10^{16}$ cm^{-3} on the anode side of the barrier. The excellent symmetry in the experimental static C-V characteristics and the discrepancy between theory and experiment at negative biases, however, indicates that the asymmetry in the experimental d.c. I-V curves may be partially due to different heterointerface barrier heights rather than solely due to asymmetry in the modulation layer doping profiles. Furthermore, the slight discrepancy between the experimental and simulated static C-V characteristics at low biases is attributed to an inaccurate barrier doping level and/or an

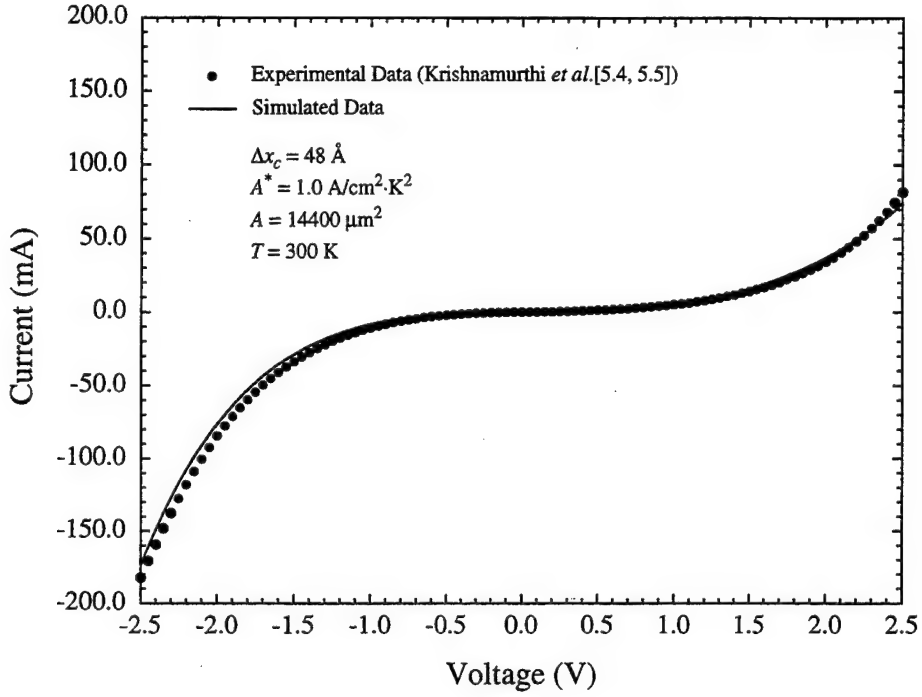

Figure 5.5 Experimental and theoretical d.c. I-V characteristics for the 120 µm diameter, circular mesa-isolated single barrier *n* GaAs/ *i* GaAs/*i* $Al_{0.4}Ga_{0.6}As$ HBVs of references [5.4] and [5.5].

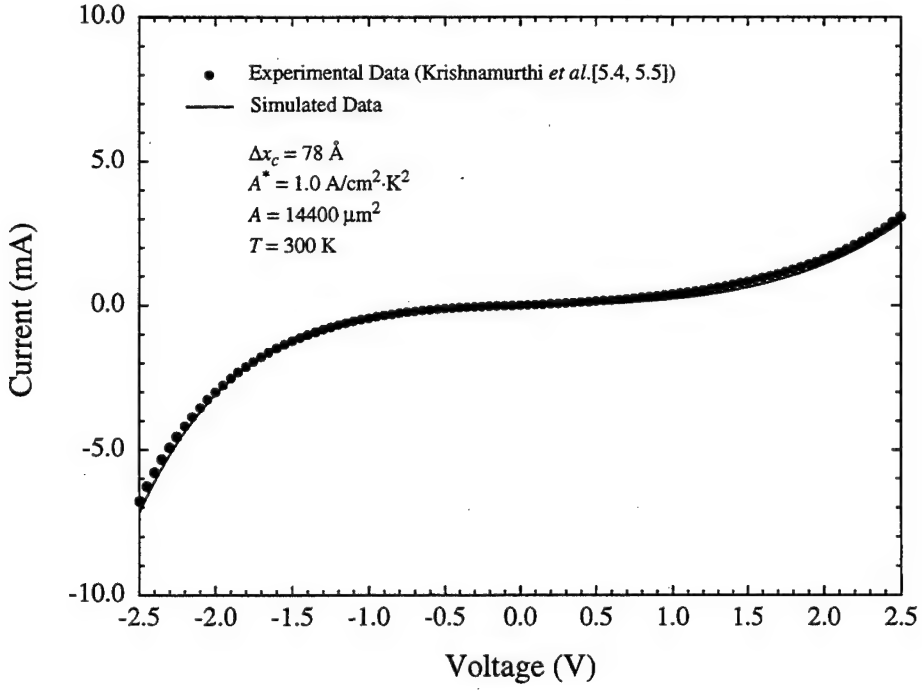

Figure 5.6 Experimental and theoretical d.c. I-V characteristics for the 120 µm diameter, circular mesa-isolated single barrier *n* GaAs/ *i* $In_{0.2}Ga_{0.8}As$/*i* $Al_{0.4}Ga_{0.6}As$ HBVs of references [5.4] and [5.5].

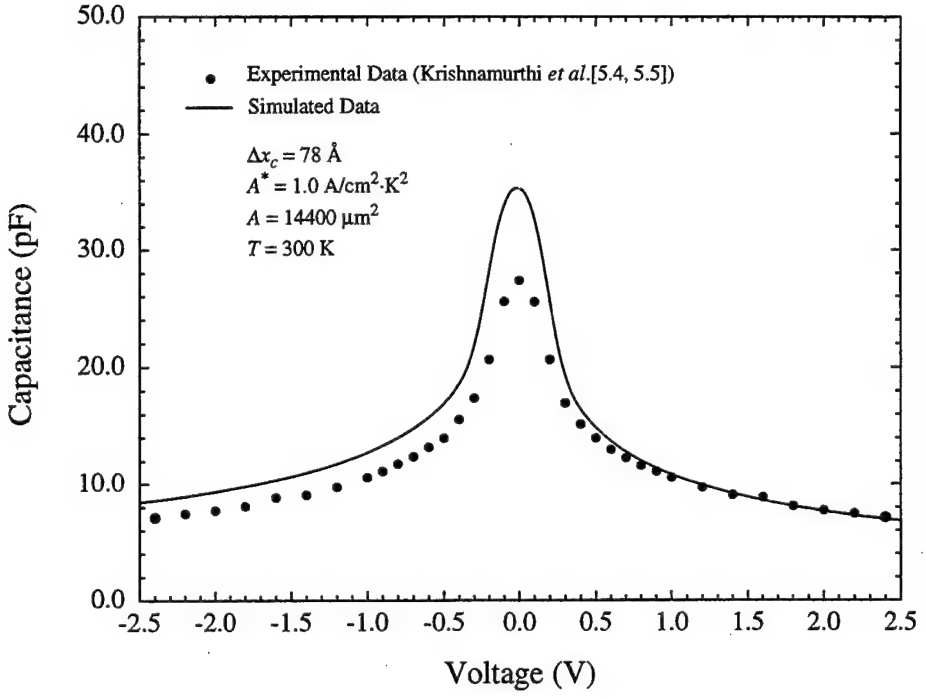

Figure 5.7 Experimental and theoretical static C-V characteristics for the 120 μm diameter, circular mesa-isolated single barrier *n* GaAs/ *i* $In_{0.2}Ga_{0.8}As$/*i* $Al_{0.4}Ga_{0.6}As$ HBVs of references [5.4] and [5.5].

inaccurate barrier width since the barrier is depleted first (at small d.c. biases) and, thus, controls the low-bias C-V relationship. In addition to the transport parameters shown in Figures 5.5-5.7, a drifted-Maxwellian electron effective mass ratio ($m^*_{D\text{-}M}/m_0$) of 0.0804 was used in the simulations. Furthermore, the current prefactor utilized here agrees with the results of Solomon *et al.*[5.1] for $Al_{0.4}Ga_{0.6}As$ barriers.

A comparison of the experimental current densities for the GaAs/$Al_{0.7}Ga_{0.3}As$, GaAs/$Al_{0.4}Ga_{0.6}As$, and GaAs/$In_{0.2}Ga_{0.8}As$/$Al_{0.4}Ga_{0.6}As$ HBVs indicates that minimal reduction in conduction current is obtained by using $Al_{0.4}Ga_{0.6}As$ rather than $Al_{0.7}Ga_{0.3}As$ barriers even though the heterointerface barrier height is slightly larger for an $Al_{0.4}Ga_{0.6}As$ barrier (see Table B.3). This is particularly evident by comparing the I-V curve of Figure 5.4 with the reverse bias I-V curve of Figure 5.5 since the modulation layer doping levels controlling these results are comparable. Furthermore, a comparison of Figures 5.5 and 5.6 shows that the use of pseudomorphic $In_{0.2}Ga_{0.8}As$ spacer layers significantly reduces the conduction current. Simulations indicate that further reduction in

conduction current can be obtained by using GaAs/500 Å graded pseudomorphic $In_{0.0\text{-}0.2}Ga_{1.0\text{-}0.8}As$ modulation layers and pseudomorphic $In_{0.2}Ga_{0.8}As$ spacer layers.

5.2 Large-Signal Time-Dependent Simulation Results

In order to investigate the importance of using numerical device simulators in place of the usual lumped quasi-static equivalent circuit device models, the harmonic-balance circuit analysis has been coupled to both the HBV and SBV numerical device simulators and simple quasi-static device models for HBVs and SBVs. The quasi-static equivalent circuit models utilize curve-fits to the d.c. I-V and static C-V characteristics of the devices as determined by the field-independent numerical device simulators. The total device current as an instantaneous function of bias, $i(V(t))$, is, thus,

$$i(V(t)) = I_{d.c.}(V(t)) + C_{static}(V(t))\frac{dV}{dt}. \tag{5.1}$$

While not completely self-consistent and certainly subject to high frequency and high power divergence problems, these quasi-static device models alleviate some of the inaccuracies associated with the device models typically employed in the analysis of frequency multipliers. One such problem is the inaccurate forward bias C-V relationship typically used to describe SBVs operating in a hybrid varactor/varistor mode, that is at high frequencies and/or high drive levels. For devices such as the HBV, the use of curve-fit device models is invaluable since the terminal characteristics of such devices are not directly amenable to description by simple analytical expressions. As will be shown below, these vastly improved quasi-static device models still lack complete self-consistency, and do not accurately model the large-signal nonstationary dynamics of carrier transport that dominate device operation at high frequencies and high drive levels.

In the remainder of this chapter, three specific whisker-contacted frequency multipliers are examined, the UVA 6P4 and UVA 5T1 GaAs SBV doublers of reference [5.6], and the single barrier $GaAs/Al_{0.7}Ga_{0.3}As$ HBV tripler of reference [5.7]. The 6P4 SBV has a 1.0 μm, $3.5x10^{16}$ cm^{-3} active region, while the 5T1 SBV has a 0.6 μm active region doped at $1.0x10^{17}$ cm^{-3}. The measured forward d.c. bias parasitic resistance

of the 6P4 (5T1) SBV is 9.5 (5.3) Ω, while the measured zero-bias capacitance is 20.0 (22.0) fF and the measured breakdown voltage is -20.0 (-10.0) V. Again, the quasi-static equivalent circuit device model for the SBVs utilized curve-fits to the static C-V characteristics as determined by the SBV numerical device simulator. The static C-V results obtained from the numerical device simulator for the 6P4 SBV are shown in Figure 5.8 along with the results obtained from the quasi-static equivalent circuit model. Likewise, Figure 5.9 shows a comparison of the 6P4 SBV d.c. I-V results obtained from the numerical device and quasi-static equivalent circuit models. For the d.c. I-V characteristics, the quasi-static equivalent circuit model actually utilized the nonlinear diode equation

$$I = I_{sat}\left[\exp\left(\frac{q(V-IR_p)}{\eta kT}\right)-1\right] \tag{5.2}$$

which was solved analytically following the technique of reference [5.8]. In this equation, the ideality factor, η, was taken to be unity, the saturation current, I_{sat}, was taken to be $5.0x10^{-17}$ A, and the parasitic resistance, R_p, was taken to be the calculated resistance of the entire SBV epitaxial layer based on the active layer electron mobility utilized in the numerical device simulator. For the 6P4 SBV, the parasitic resistance was 10.89 Ω based on a mobility of 4950 $cm^2/V{\cdot}s$; for the 5T1 SBV, the resistance was 4.36 Ω based on a mobility of 4200 $cm^2/V{\cdot}s$. A metal-semiconductor barrier height, ϕ_b, of 1.0 V was used in the numerical device simulator for both SBVs. It is important to note that no parasitic resistance term was used in obtaining the numerical device simulator d.c. I-V results; the correctly simulated linear I-V characteristic in high forward bias is a direct consequence of the resistive nature of a Schottky diode above the flat-band voltage. Furthermore, it should be noted that the forward bias static C-V characteristic of the SBV is properly simulated[5.9] as a consequence of using the current density-dependent surface recombination velocity in the Schottky contact current boundary constraint[5.10, 5.11].

The Choudhury *et al.*[5.7] HBV that has been investigated consists of a 213 Å intrinsic $Al_{0.7}Ga_{0.3}As$ barrier surrounded by 53 Å intrinsic GaAs spacer layers and 5330 Å *n*-type ($1x10^{17}$ cm^{-3}) GaAs modulation layers. The slight asymmetry evident in the experimental HBV data has been modeled via a slight asymmetry in the modulation layer

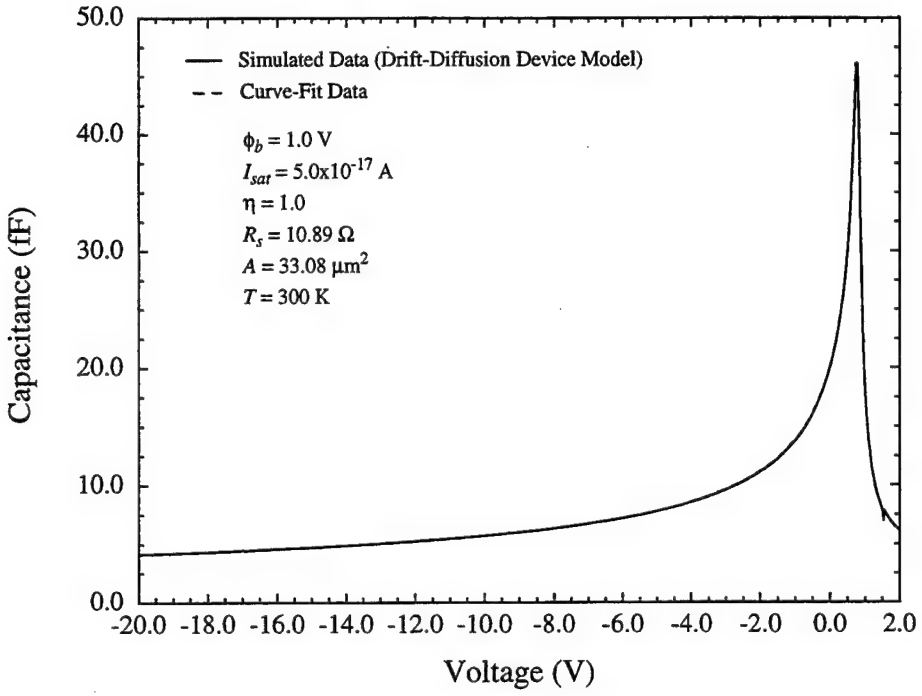

Figure 5.8 Simulated and curve-fit C(V) characteristics for the UVA 6P4 GaAs SBV of reference [5.6].

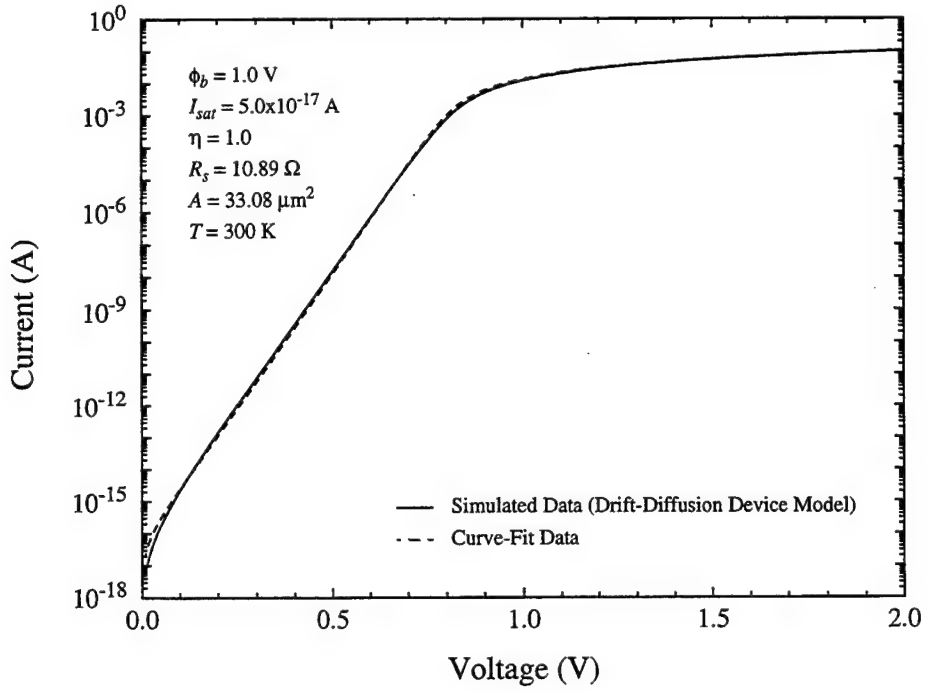

Figure 5.9 Simulated and curve-fit I(V) characteristics for the UVA 6P4 GaAs SBV of reference [5.6].

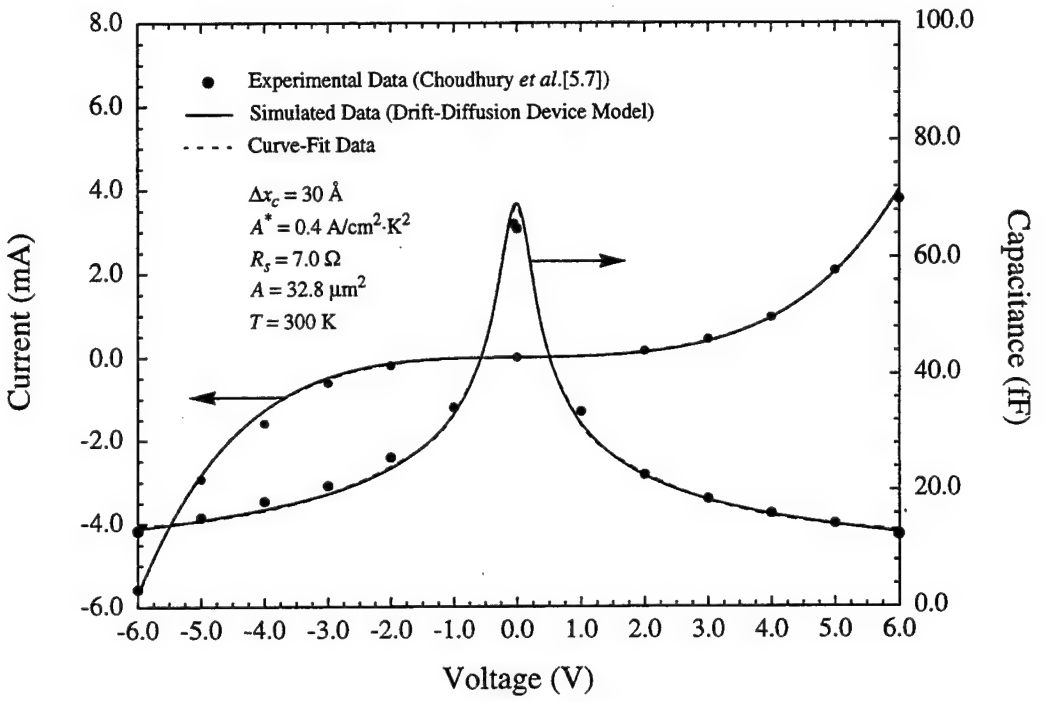

Figure 5.10 Experimental, simulated, and curve-fit I(V) and C(V) characteristics for the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7].

doping concentrations; one side of the device was assumed to have a doping concentration of $1.0x10^{17}$ cm^{-3}, while the other side was assumed to have a doping concentration of $1.125x10^{17}$ cm^{-3}. In the numerical device simulator, an effective Richardson constant of 0.4 A/cm^{2}K^2 was assumed for the heterointerface current density boundary constraints, and a drifted-Maxwellian electron effective mass ratio ($m^*_{D\text{-}M}/m_0$) of 0.6115 was used. The quasi-static equivalent circuit model for this HBV was derived entirely from curve-fits to the d.c. I-V and static C-V results obtained from the numerical device simulator. As expected from the results of *Section 5.1*, excellent correlation has been obtained between the HBV numerical device simulator and the experimental d.c. I-V and static C-V characteristics of reference [5.7]. Figure 5.10 shows the experimental results for this HBV along with the simulated characteristics from the quasi-static equivalent circuit device and numerical device models. The measured parasitic resistance of 7.0 Ω has been utilized in calculating the simulated and curve-fit d.c. I-V and static C-V characteristics. Unlike the measured 6P4 SBV resistance, this measured HBV resistance is primarily due to parasitic

resistances external to the active region of the simulated device and is, thus, not accounted for in the numerical device simulator.

5.2.1 Large-Signal Sinusoidal Results

Although the voltage waveform seen by an HBV or SBV multiplier will not, in general, be a pure sinusoid due to the interaction between the nonlinear device and its embedding circuit, it is still instructive to examine how HBV and SBV diodes respond to a pure sinusoidal large-signal voltage excitation. Fourier analysis of the applied voltage waveform and the resulting current waveform can be utilized to obtain information about the fundamental and harmonic frequency components of the voltage and current, as well as about the complex device impedance at the fundamental frequency. By comparing large-signal sinusoidal simulation results from the quasi-static equivalent circuit and numerical device models, it is possible to examine the frequencies and drive levels at which the lumped quasi-static device models diverge from the numerical device models on which they are based. More importantly, these large-signal sinusoidal comparisons make it possible to elucidate the physical phenomena underlying the differences between these two device modeling approaches. Numerical device/harmonic-balance circuit simulations, which properly model device parasitic impedances and correctly account for the interaction between the nonlinear device and its embedding circuit, will be presented in a subsequent section of this chapter.

5.2.1.1 Comparison of Results for GaAs/AlGaAs and GaAs/InGaAs/AlGaAs HBV Device Structures

Before comparing large-signal sinusoidal simulation results from the quasi-static equivalent circuit and numerical device models, large-signal sinusoidal results for two candidate HBV device structures will be examined. Figure 5.11 shows the current waveforms for single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ and GaAs/$In_{0.0\text{-}0.2}Ga_{1.0\text{-}0.8}As$/$Al_{0.7}Ga_{0.3}As$ HBV devices, with anode diameters of 8 μm, subject to a 100 GHz, 1.0 V sinusoidal excitation. Both HBVs had a 200 Å undoped $Al_{0.7}Ga_{0.3}As$ barrier surrounded by 50 Å undoped spacer layers and 3500 Å *n*-type ($1x10^{17}$ cm^{-3}) modulation layers. The GaAs/AlGaAs structure had GaAs spacer and

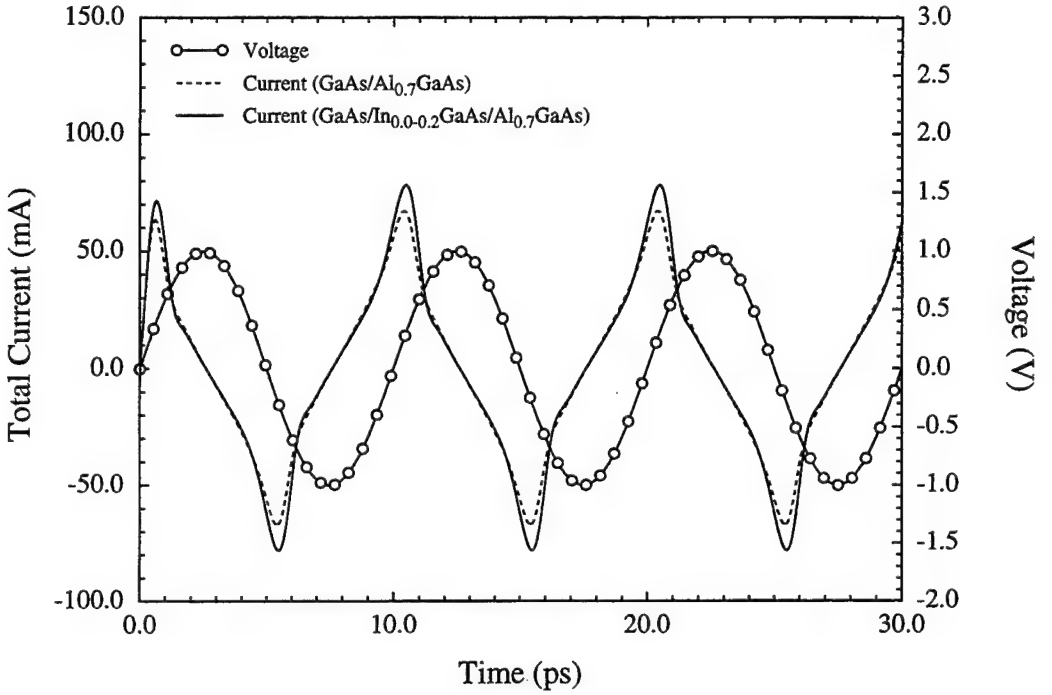

Figure 5.11 Theoretical current waveforms for 8 μm diameter, circular single barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ and *n* GaAs/*n* $In_{0.0\text{-}0.2}Ga_{1.0\text{-}0.8}As$/ *i* $In_{0.2}Ga_{0.8}As$/*i* $Al_{0.7}Ga_{0.3}As$ HBVs d.c. biased at 0.0 V and subject to 100 GHz, 1.0 V sinusoidal excitation.

modulation layers, while the GaAs/InGaAs/AlGaAs structure had 3000 Å GaAs/500 Å graded pseudomorphic $In_{0.0\text{-}0.2}Ga_{1.0\text{-}0.8}As$ modulation layers and pseudomorphic $In_{0.2}Ga_{0.8}As$ spacer layers. Under such an excitation, the impedance of the 8 μm single barrier GaAs/AlGaAs device was $Z(f_1=100\text{ GHz}) = 2.288 - j20.496\ \Omega$; for the 8 μm single barrier GaAs/InGaAs/AlGaAs device, the impedance was $Z(f_1=100\text{ GHz}) = 2.467 - j18.731\ \Omega$. For similar four barrier HBV structures, the impedances become four times larger.

In terms of the harmonic content of the output current waveforms, the even-harmonic components are negligible when compared to the components of the odd-harmonic frequencies, as expected. This is especially clear from Figure 5.11 where the current waveforms are triangular in shape and, thus, primarily composed of odd harmonics. For the 8 μm GaAs/AlGaAs device, the ratio of the current magnitude at $3f_1$ to that at f_1 is approximately 0.222; for the 8 μm GaAs/InGaAs/AlGaAs device, this ratio is

approximately 0.289. More importantly, the current magnitude at $3f_1$ is 5.388 mA for the GaAs/AlGaAs device and increases to 7.657 mA for the GaAs/InGaAs/AlGaAs device, an increase of about 42 % in the third harmonic component of the current waveform. Overall, the results given here for HBVs subject to a pure sinusoidal large-signal excitation indicate that the GaAs/InGaAs/AlGaAs HBV should provide enhanced tripler performance when compared to the performance of the GaAs/AlGaAs HBV. Although the improved performance is rather modest based on the large-signal sinusoidal simulations, full harmonic-balance simulations of these two devices indicate that the GaAs/InGaAs/AlGaAs HBV should provide at least 1.4 times the output power at an available pump power of 20 mW at 64 GHz when compared to the GaAs/AlGaAs HBV. The improved performance is a direct consequence of reduced conduction current and improved capacitance modulation (increased maximum to minimum ratio and sharpness).

5.2.1.2 Comparison of Results From Quasi-Static Equivalent Circuit and Numerical Device Models

Figures 5.12-5.17 show the current and voltage waveforms for the 6P4 SBV d.c. biased at -9.0 V and subject to a 10.0 V sinusoidal excitation voltage at 1 GHz, 10 GHz, 50 GHz, 100 GHz, 200 GHz, and 300 GHz, respectively. Likewise, Figures 5.18-5.23 show the current and voltage waveforms for the Choudhury *et al.* HBV d.c. biased at 0.0 V and subject to a 2.0 V sinusoidal excitation voltage at 1 GHz, 10 GHz, 50 GHz, 100 GHz, 200 GHz, and 300 GHz, respectively. For the 6P4 SBV subject to the specified drive level, the current waveforms from the two device models begin to deviate at about 50 GHz with the deviations increasing with increasing frequency. For the Choudhury *et al.* HBV subject to the specified drive level, the current waveforms from the two device models begin to deviate at about 10 GHz with the deviations, again, increasing with increasing frequency.

At low frequencies (below about 10 GHz in the SBV and about 1 GHz in the HBV), when the current throughout the device is dominated by conduction current, small discrepancies between the results of the two models are observed. These discrepancies are attributed to small errors in the curve-fits to the numerical device d.c. I-V results. At higher frequencies, the current is dominated by displacement current in high field regions of the device (near the Schottky barrier or heterostructure barrier) and by conduction current in

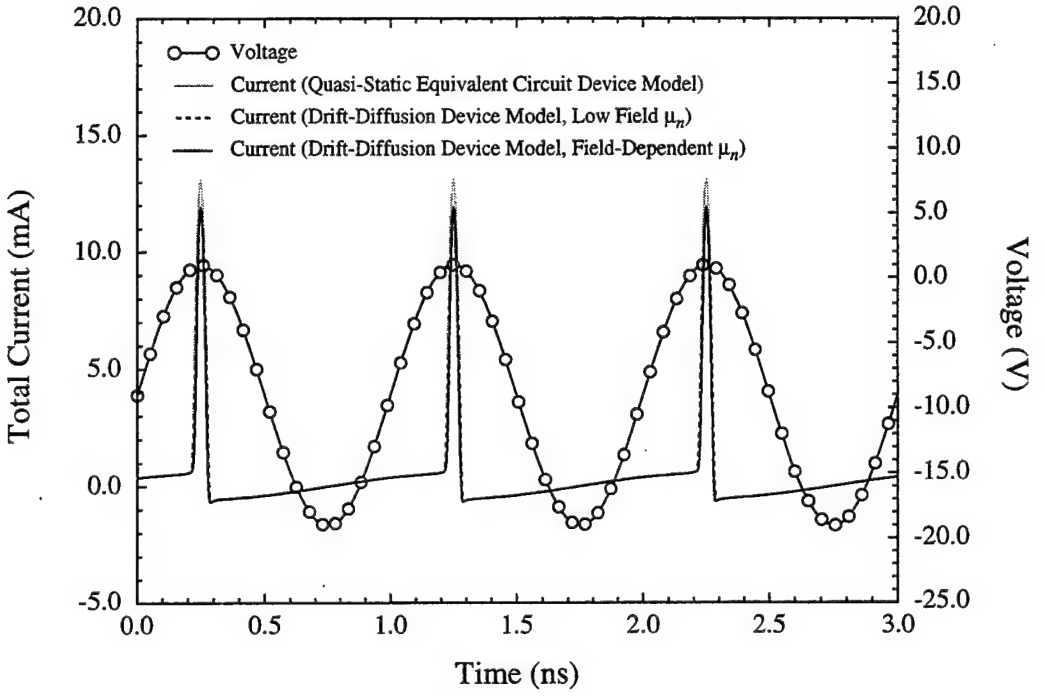

Figure 5.12 Theoretical current waveforms for the UVA 6P4 GaAs SBV of reference [5.6] d.c. biased at -9.0 V and subject to 1 GHz, 10.0 V sinusoidal excitation.

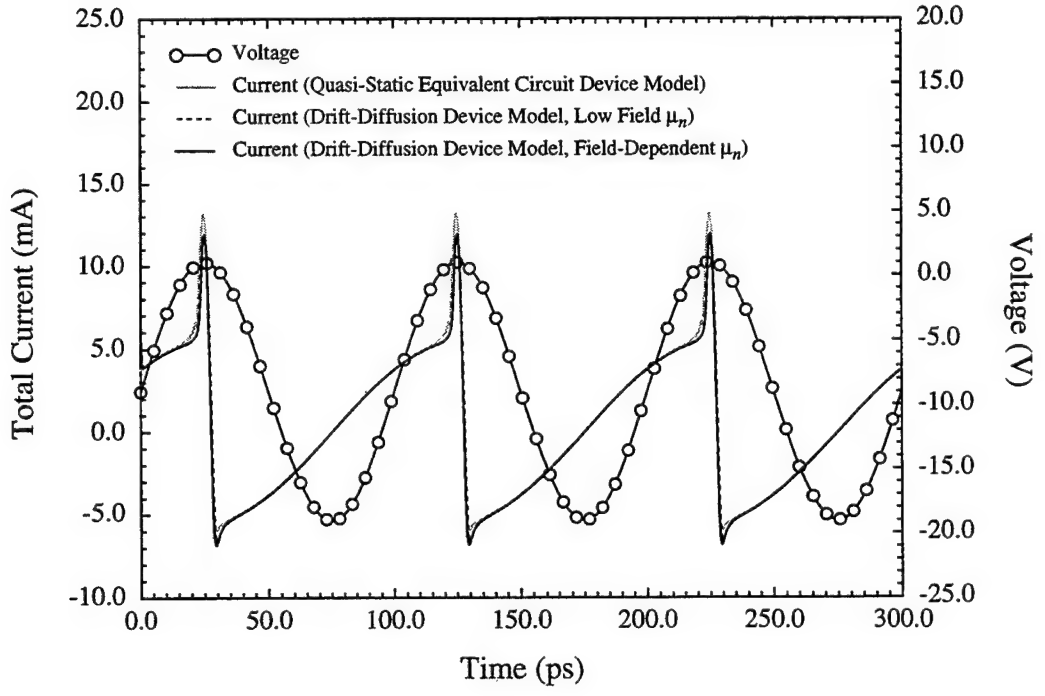

Figure 5.13 Theoretical current waveforms for the UVA 6P4 GaAs SBV of reference [5.6] d.c. biased at -9.0 V and subject to 10 GHz, 10.0 V sinusoidal excitation.

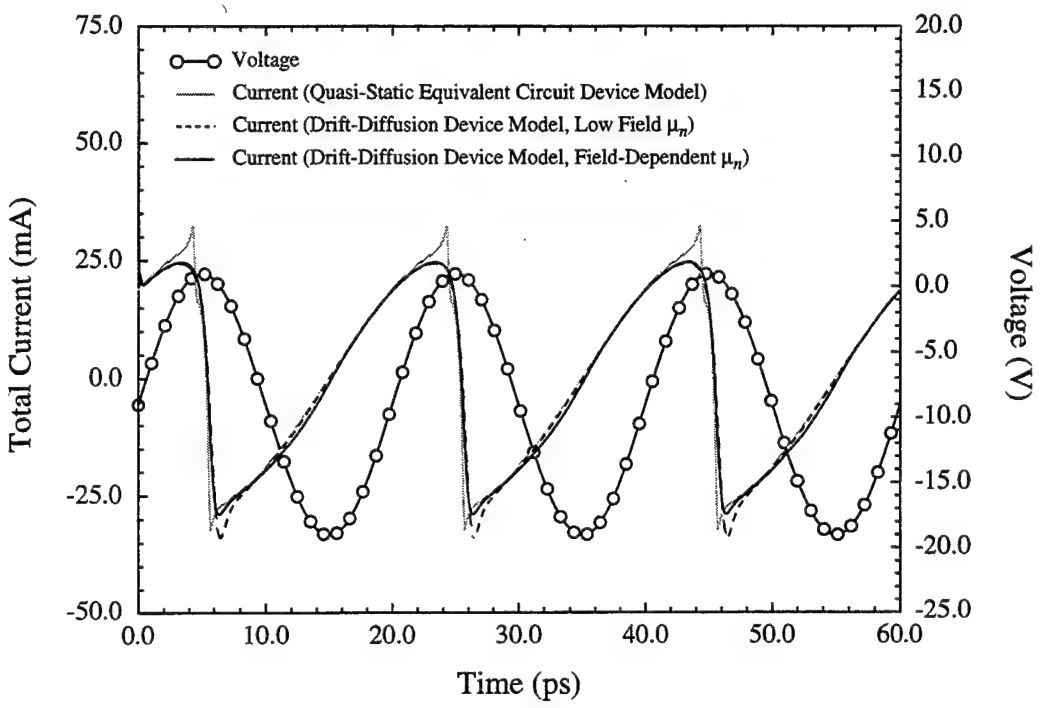

Figure 5.14 Theoretical current waveforms for the UVA 6P4 GaAs SBV of reference [5.6] d.c. biased at -9.0 V and subject to 50 GHz, 10.0 V sinusoidal excitation.

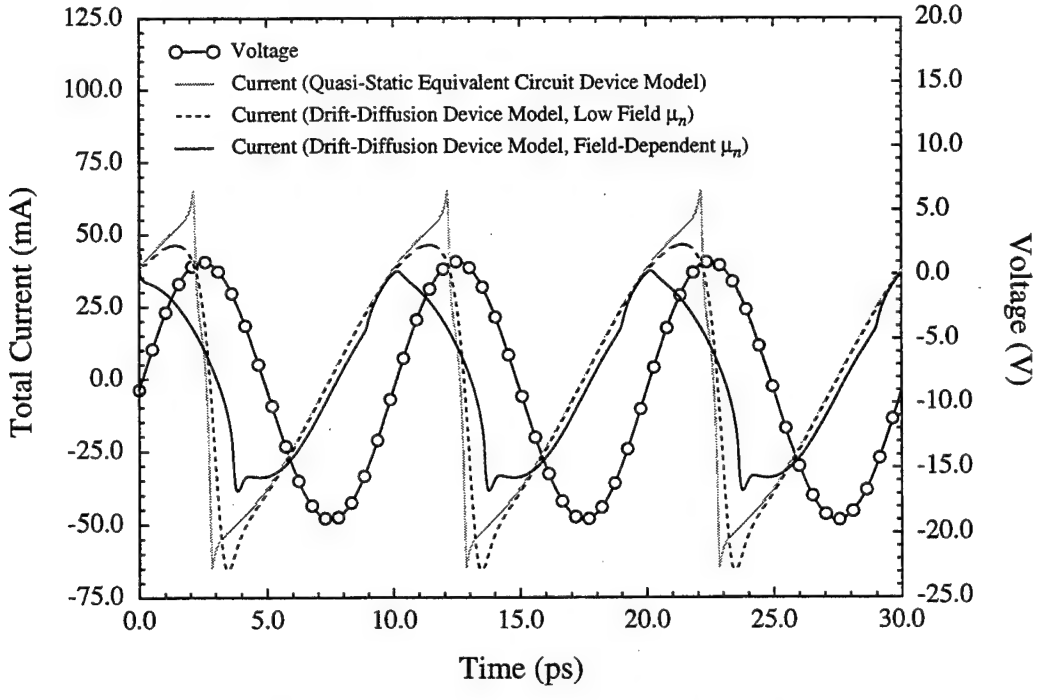

Figure 5.15 Theoretical current waveforms for the UVA 6P4 GaAs SBV of reference [5.6] d.c. biased at -9.0 V and subject to 100 GHz, 10.0 V sinusoidal excitation.

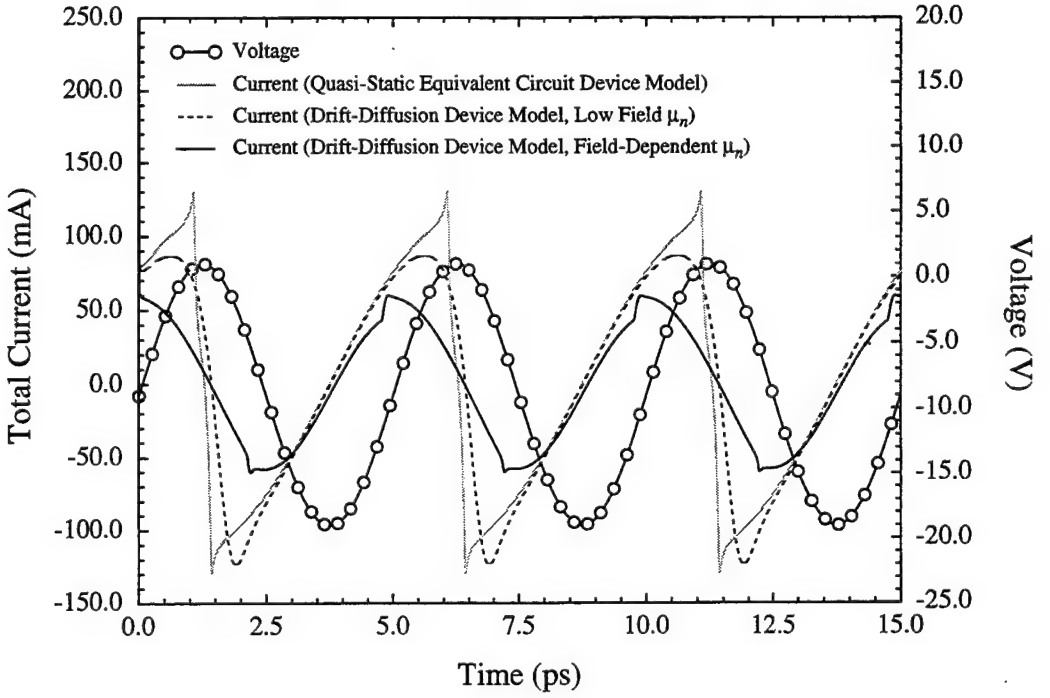

Figure 5.16 Theoretical current waveforms for the UVA 6P4 GaAs SBV of reference [5.6] d.c. biased at -9.0 V and subject to 200 GHz, 10.0 V sinusoidal excitation.

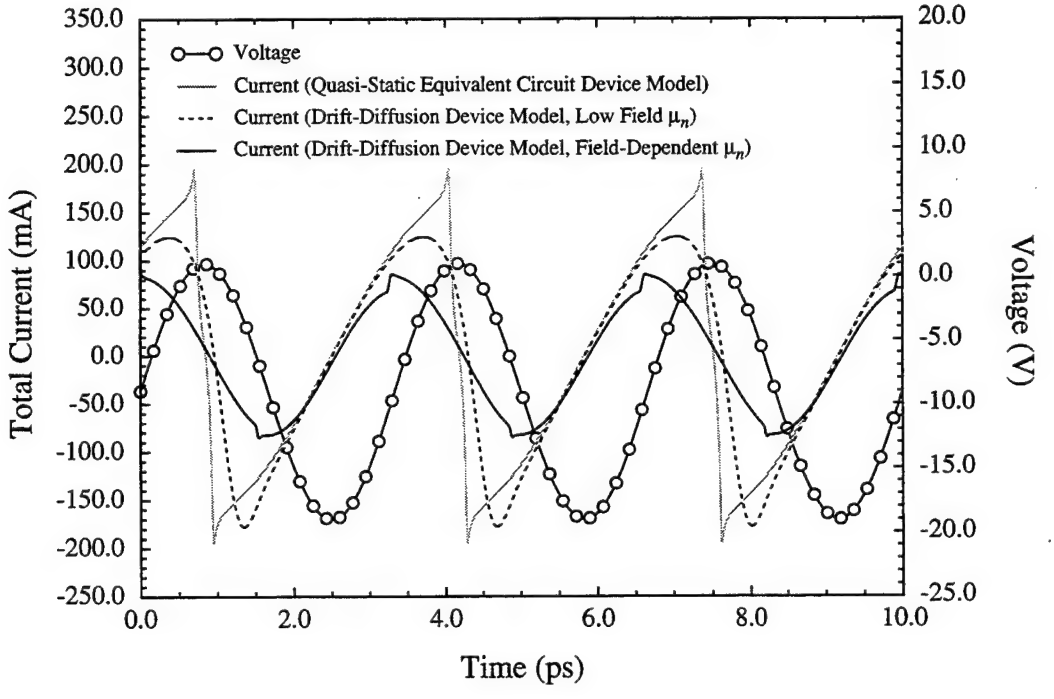

Figure 5.17 Theoretical current waveforms for the UVA 6P4 GaAs SBV of reference [5.6] d.c. biased at -9.0 V and subject to 300 GHz, 10.0 V sinusoidal excitation.

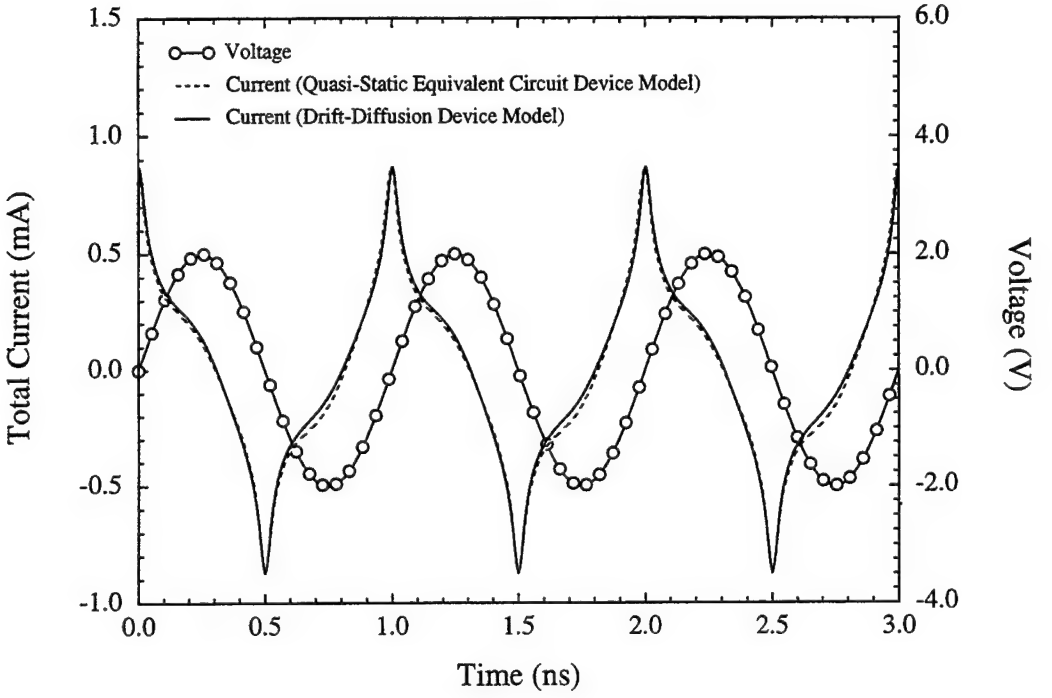

Figure 5.18 Theoretical current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and subject to 1 GHz, 2.0 V sinusoidal excitation.

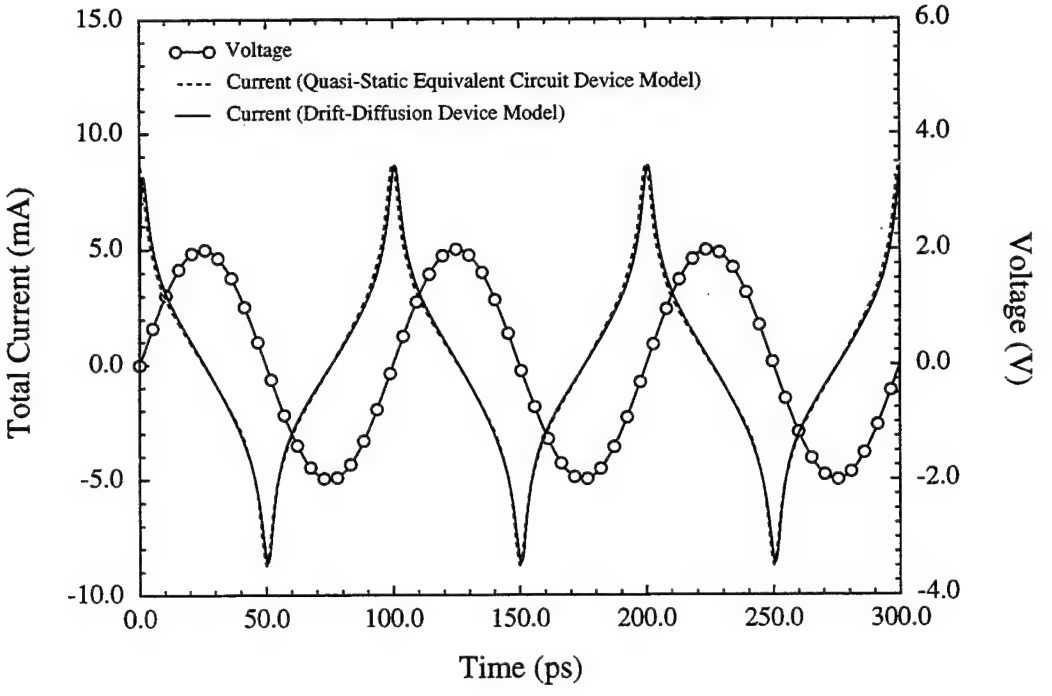

Figure 5.19 Theoretical current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and subject to 10 GHz, 2.0 V sinusoidal excitation.

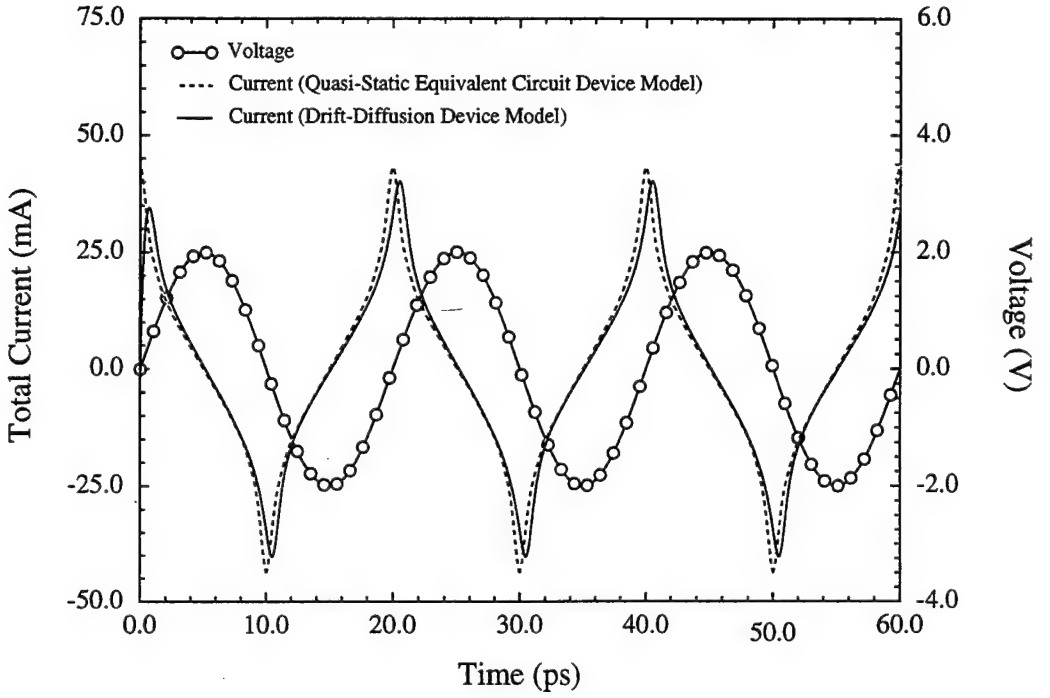

Figure 5.20 Theoretical current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and subject to 50 GHz, 2.0 V sinusoidal excitation.

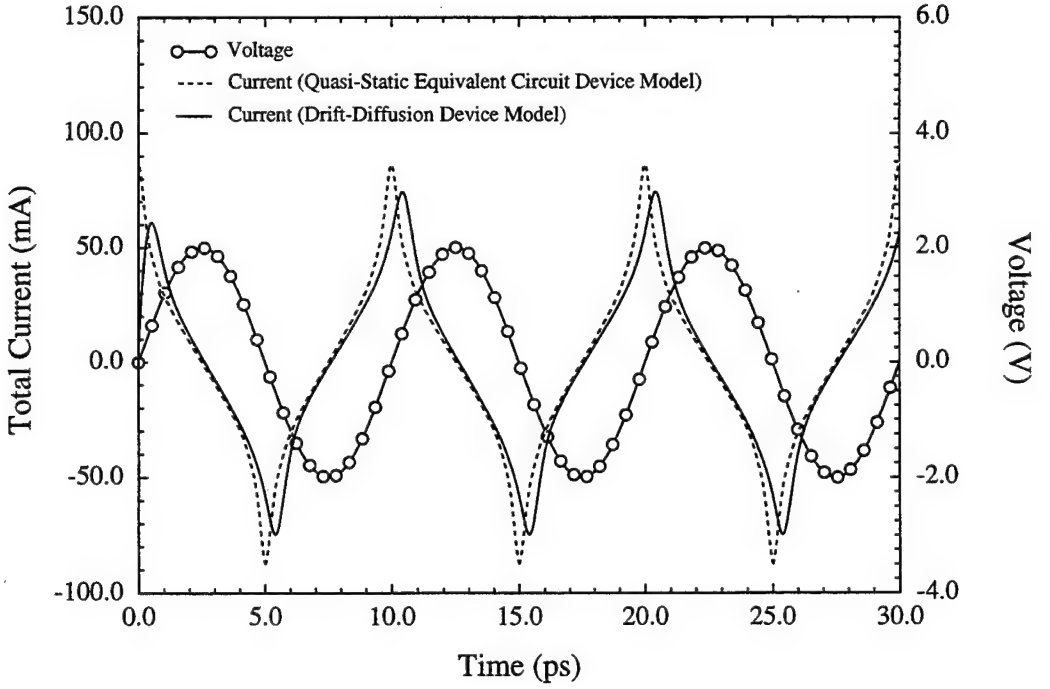

Figure 5.21 Theoretical current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and subject to 100 GHz, 2.0 V sinusoidal excitation.

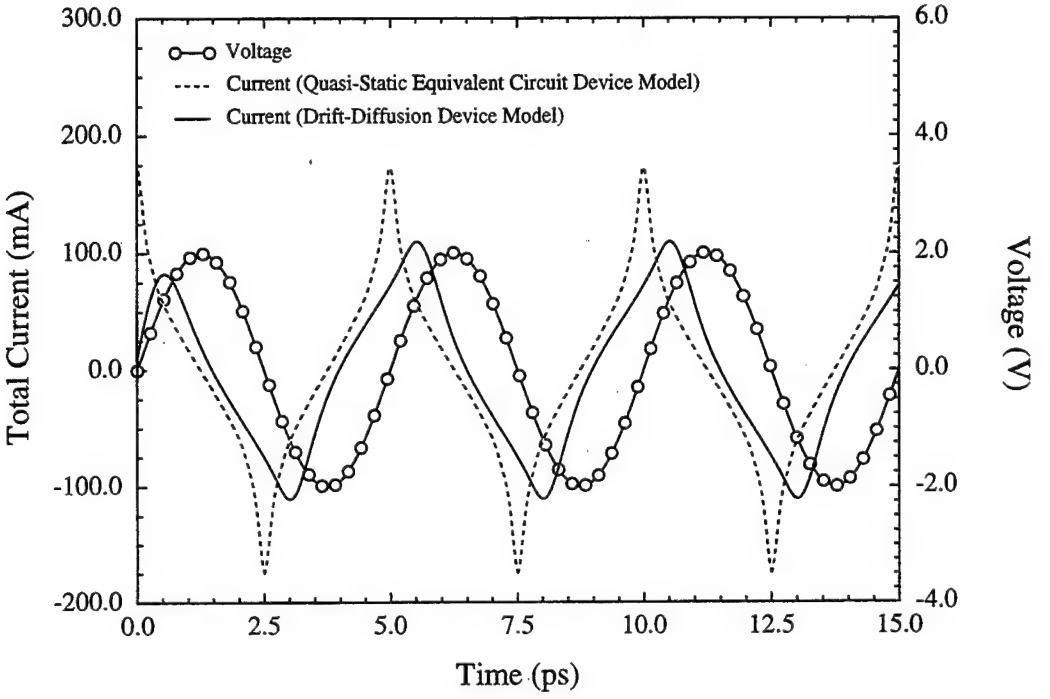

Figure 5.22 Theoretical current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and subject to 200 GHz, 2.0 V sinusoidal excitation.

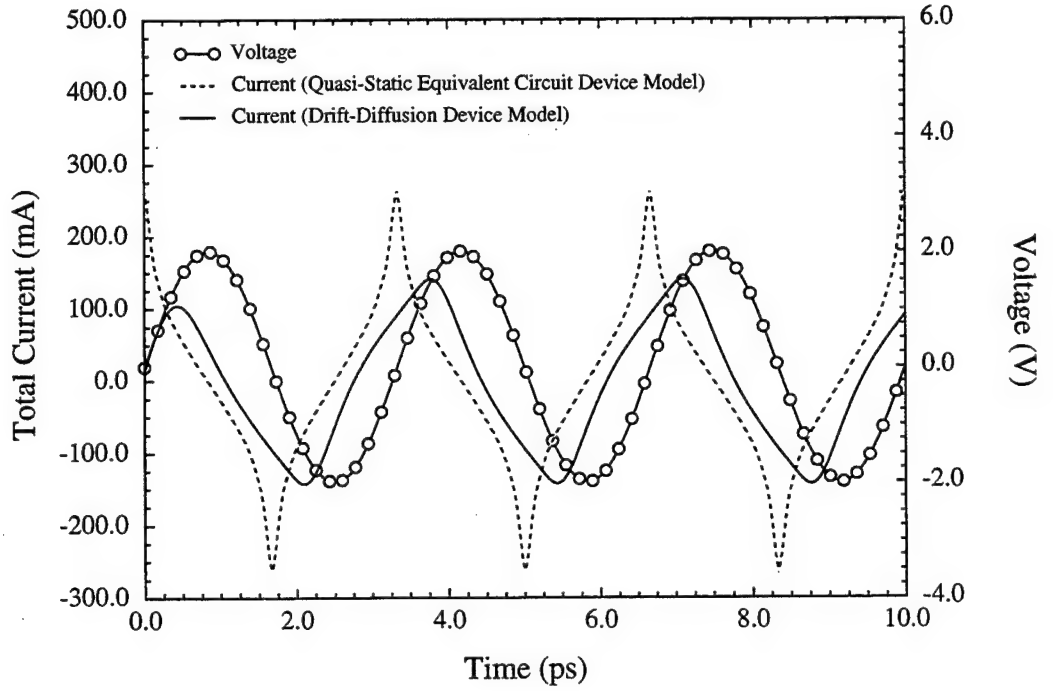

Figure 5.23 Theoretical current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and subject to 300 GHz, 2.0 V sinusoidal excitation.

low field regions of the device (near the ohmic contacts). In the numerical device simulator, the conduction and displacement currents are balanced throughout the device in a self-consistent manner so that the total current versus position is constant. In the quasi-static equivalent circuit model, however, these currents are not self-consistently balanced. As a result, the displacement current in the high field regions of the device can greatly exceed the sustainable conduction current in the (relatively) low field regions of the device. As a result, the increasing current waveform deviations that have been observed with increasing frequency are a direct consequence of the current saturation phenomenon described in references [5.12] and [5.6]. These deviations also increase with increasing drive level. Although attempts have been made to compensate for this lack of self-consistency in the quasi-static equivalent circuit models[5.13, 5.14], the resulting models are device-specific, and require empirical fitting parameters and/or an analytical understanding of the device's internal physics.

In essence, the standard quasi-static equivalent circuit device models assume an infinite electron mobility such that there is no limit to the allowable displacement current in the device. To further examine this concept, the quasi-static equivalent circuit device models for the 6P4 SBV and the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV have been compared with their respective numerical device models assuming an active region electron mobility of μ_{n0}, twice μ_{n0}, and one half μ_{n0}. For the 6P4 SBV, $\mu_{n0} = 4950$ cm^2/V·s; for the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV, $\mu_{n0} = 4200$ cm^2/V·s. The results are shown in Figures 5.24 and 5.25 for drive levels identical to those previously specified. Clearly, as the active region mobility is increased from μ_{n0}, the current waveform from the numerical device simulator approaches that of the quasi-static equivalent circuit model. Alternately, as the active region mobility is decreased from μ_{n0}, the differences between the numerical device simulator current waveform and that of the quasi-static equivalent circuit model increase.

It is important to remember that the phenomenon described above is strictly a current saturation phenomenon. Since a constant, field-independent electron mobility has been utilized, saturation of the electron drift-velocity has not been accounted for. For relatively long diodes such as the UVA 6P4 GaAs SBV, drift-velocity saturation can be

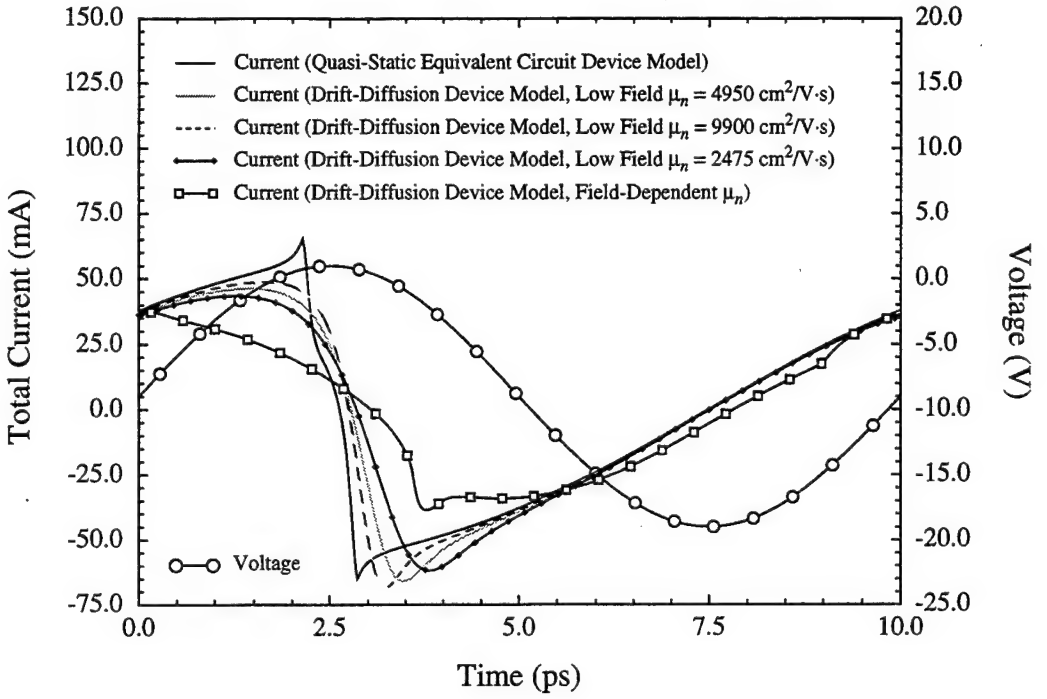

Figure 5.24 Theoretical 100 GHz current waveforms for the UVA 6P4 GaAs SBV of reference [5.6], d.c. biased at -9.0 V and subject to 10.0 V sinusoidal excitation, with varying numerical device model electron mobility.

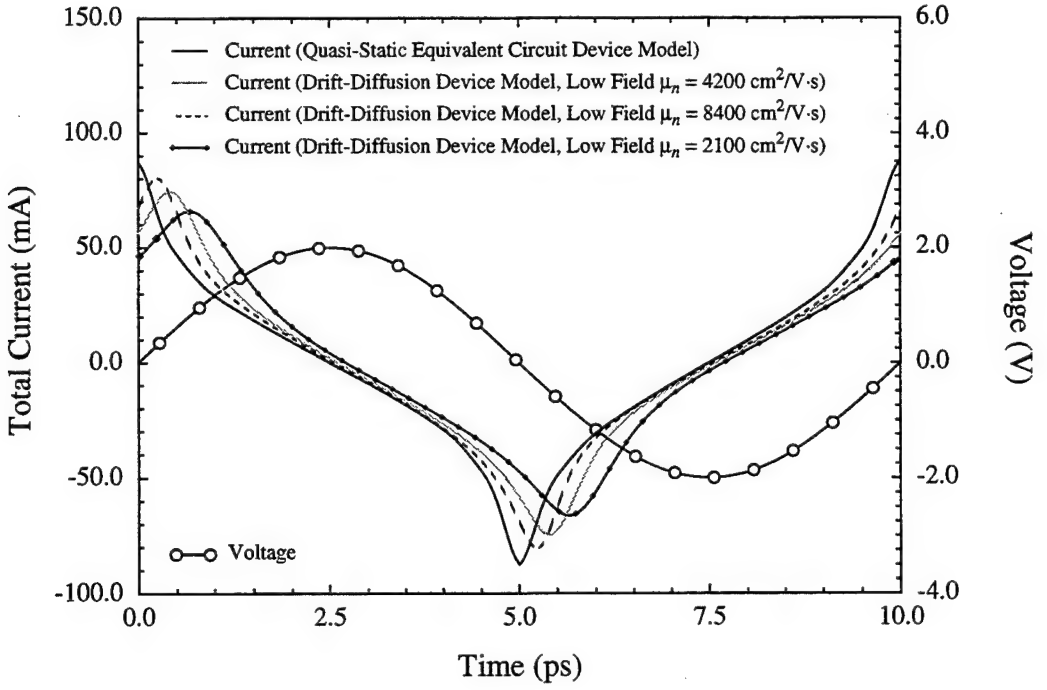

Figure 5.25 Theoretical 100 GHz current waveforms for the GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7], d.c. biased at 0.0 V and subject to 2.0 V sinusoidal excitation, with varying numerical device model electron mobility.

incorporated into the SBV numerical device model by using a field-dependent electron mobility. Figures 5.12-5.17 include 6P4 SBV results from the numerical device simulator incorporating such a field-dependent electron mobility (see Figure 2.4). From these figures, it is clear that drift-velocity saturation can have a dramatic affect on electron transport through the SBV at high frequencies; this, in turn, has a significant impact on the predicted large-signal current waveforms. Note that for relatively short diodes such as the UVA 5T1 GaAs SBV, the full momentum-balance and energy-balance equations[5.15] would have to be solved instead of the drift-diffusion equations in order to accurately account for saturation of the electron drift-velocity.

5.2.2 Harmonic-Balance Results

The differences in the sinusoidally pumped results, presented in the last section for the quasi-static equivalent circuit and numerical device models, are relatively small, at least below 100 GHz for the specified drive levels. Again, it is important to note that the differences increase with increasing frequency and drive level, and can be quite substantial above about 150 GHz (see Figures 5.16 and 5.17 and Figures 5.22 and 5.23). These relatively small differences, however, are magnified by the nonlinearity of the device when it is embedded in a circuit.

This phenomenon has been investigated, for the UVA 6P4 GaAs SBV doubler pumped at 100 GHz and the Choudhury *et al.* single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV tripler pumped at 64 GHz, using the harmonic-balance circuit analysis technique in conjunction with the quasi-static equivalent circuit and numerical device models[5.16-5.18]. To facilitate the harmonic-balance simulations, parasitic impedances for these whisker-contacted frequency multipliers, external to the active regions of the devices, have been calculated using estimated chip parameters (ohmic contact resistivities of $2x10^{-6}$ Ωcm^2, total chip thicknesses of 4 mils, and square chip side lengths of 250 μm). For the 6P4 SBV doubler pumped at 100 GHz, the d.c. impedance is 0.614 Ω and the impedances at the fundamental and second-harmonic frequencies are $1.491 + j1.016$ Ω and $1.924 + j1.549$ Ω, respectively. For the HBV tripler pumped at 64 GHz, the d.c. impedance is 7.021 Ω and the impedances at the fundamental and third-harmonic frequencies are $7.685 + j0.788$ Ω and $8.298 + j1.537$ Ω, respectively. Figure 5.26 shows the calculated

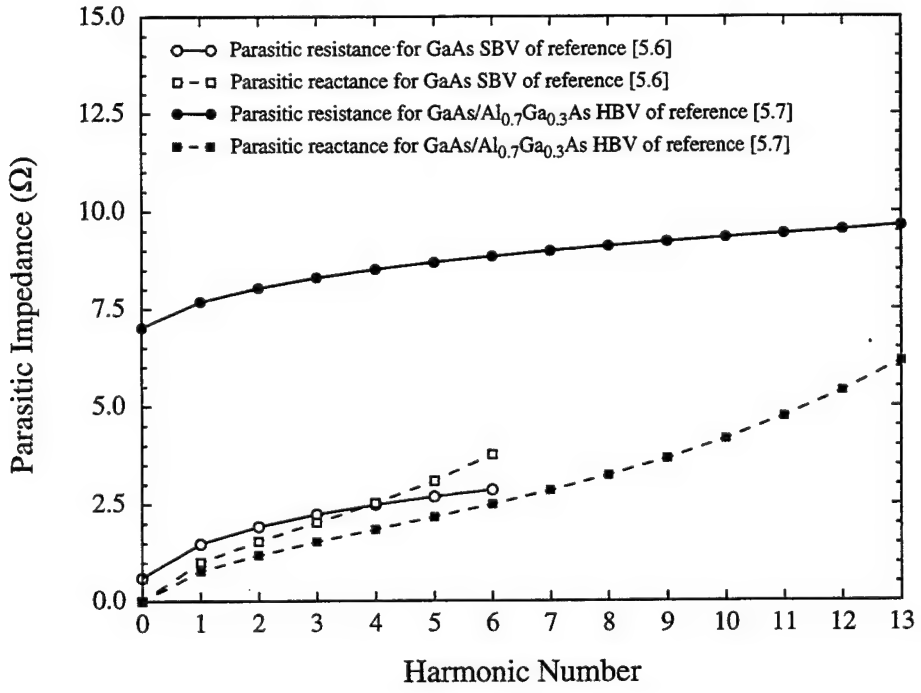

Figure 5.26 Parasitic impedances versus harmonic number for the UVA 6P4 GaAs SBV of reference [5.6] pumped at $f_1 = 100$ GHz and the single barrier GaAs/$Al_{0.7}Ga_{0.3}$As HBV of reference [5.7] pumped at $f_1 = 64$ GHz.

parasitic impedances for these two devices as a function of harmonic number; for the SBV, six harmonics plus the d.c. term have been utilized, while thirteen harmonics plus the d.c. term have been utilized for the HBV.

At the available pump powers of interest, near-optimum fundamental and third-harmonic circuit impedances for the Choudhury *et al.* HBV tripler d.c. biased at 0.0 V have been estimated from reference [5.7] for a device d.c. parasitic impedance of 7.0 Ω. The near-optimum fundamental circuit impedances vary from $8.75 + j46.75\ \Omega$ to $19.25 + j92.50\ \Omega$ for available pump powers ranging from 0 mW to 40 mW; the near-optimum third-harmonic circuit impedances vary from $10.75 + j15.75\ \Omega$ to $17.50 + j35.50\ \Omega$ over the same pump power range. Figure 5.27 shows the near-optimum fundamental and third-harmonic circuit impedances for this device across the entire available pump power range.

For the 6P4 SBV doubler, experimental d.c. bias values have been utilized[5.19]; these values are shown in Figure 5.28. Near-optimum fundamental and second-harmonic

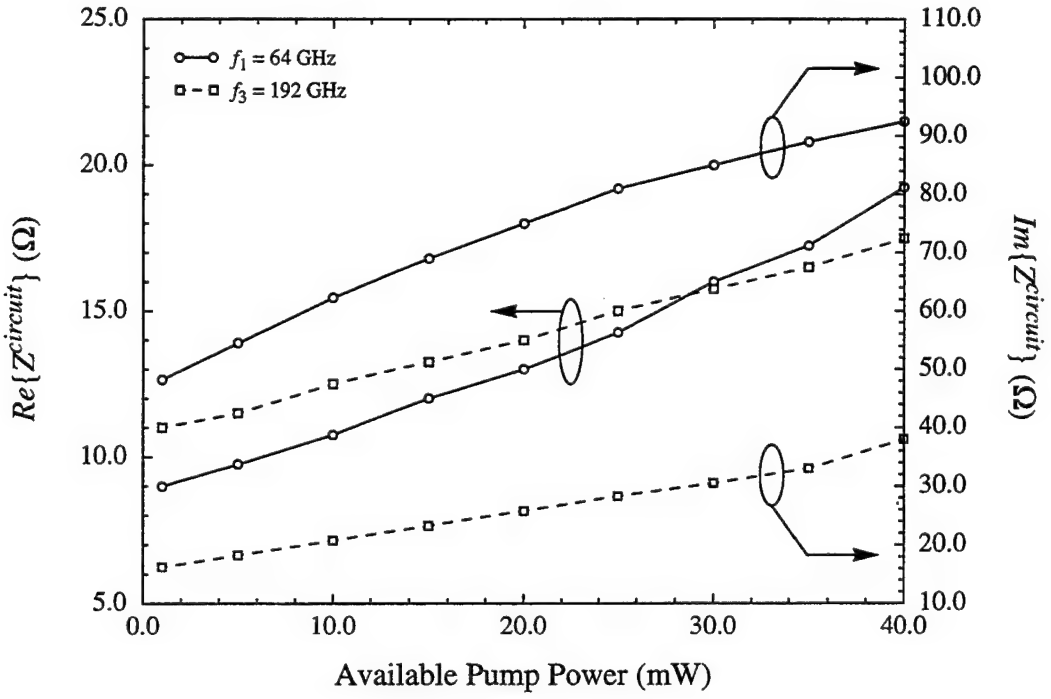

Figure 5.27 Near-optimum fundamental and third-harmonic circuit impedances versus available pump power for the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV of reference [5.7] d.c. biased at 0.0 V and pumped at f_1 = 64 GHz.

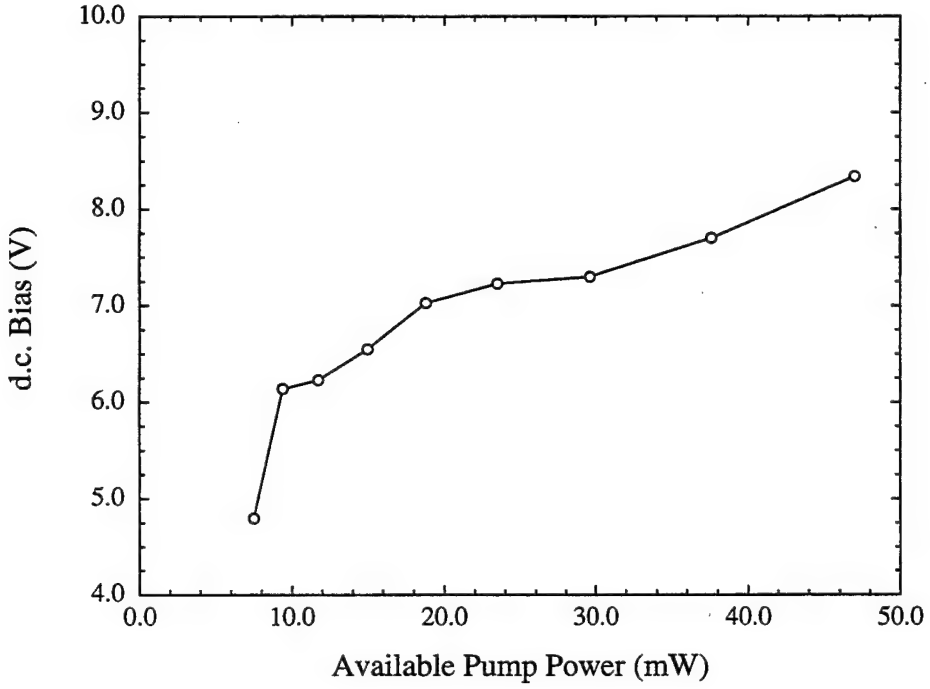

Figure 5.28 Experimental d.c. bias values versus available pump power[5.19] for the UVA 6P4 GaAs SBV reference [5.6] pumped at f_1 = 100 GHz.

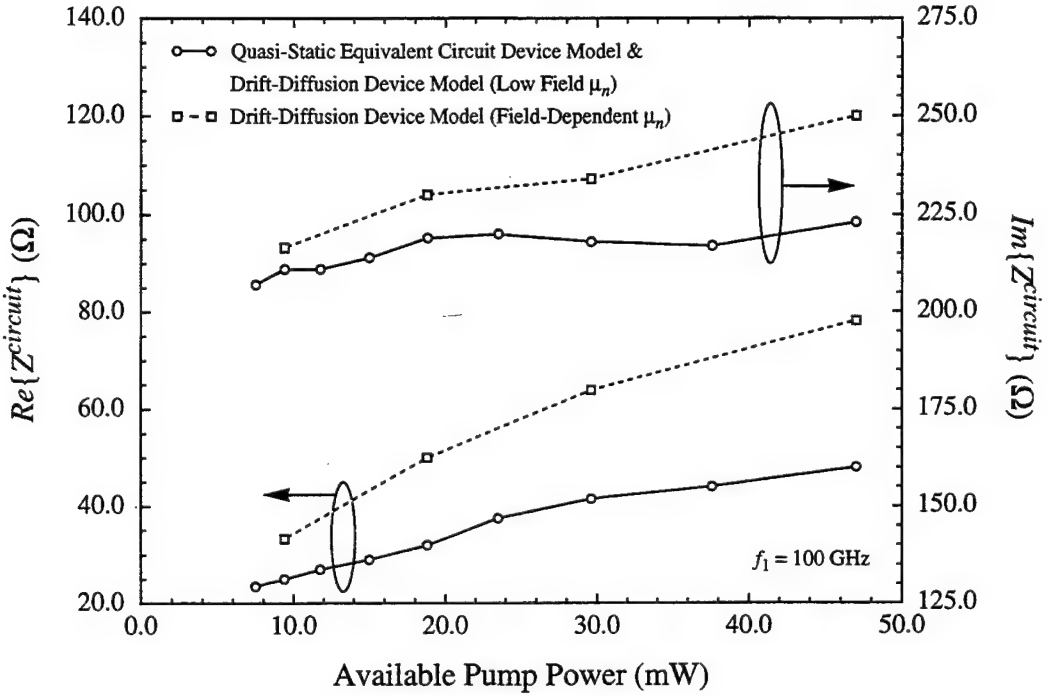

Figure 5.29 Near-optimum fundamental circuit impedances versus available pump power for the UVA 6P4 GaAs SBV of reference [5.6] pumped at $f_1 = 100$ GHz and d.c. biased as shown in Figure 5.28. Reoptimized fundamental circuit impedances are also shown for simulations using the drift-diffusion device model with field-dependent electron mobility.

circuit impedances have been obtained for this doubler from the harmonic-balance circuit simulator coupled to the quasi-static 6P4 SBV equivalent circuit device model. For simplicity, these SBV doubler circuit impedances have been optimized subject to the following constraints: (1) the real parts of the two harmonic circuit impedances are equal and (2) the imaginary part of the second-harmonic circuit impedance is half of the impedance at the fundamental. These optimization constraints are based on the assumption that the device resistance and average capacitance remain fairly constant with frequency, at least for the frequencies of interest here. As such, the optimum reactance of the embedding circuit scales nearly linearly with harmonic number. The optimized fundamental circuit impedances vary from $23.5 + j207.0\ \Omega$ to $48.0 + j223.0\ \Omega$ for available pump powers ranging from 7.5 mW to 47 mW. Figure 5.29 shows the near-optimum fundamental circuit impedances for this device across the entire available pump power range. Note that this figure includes reoptimized fundamental circuit impedances for

simulations using the drift-diffusion device model in conjunction with a field-dependent electron mobility. From these results, it is clear that the use of a field-dependent mobility has led to an increase in the average device conductance and a reduction in the average device capacitance since the near-optimum circuit resistances and reactances are larger for the field-dependent mobility simulations than they are for the field-independent (low field) simulations.

For both frequency multipliers, the high-order harmonic circuit impedances are set to short-circuit impedances of $0.001 + j0.0\ \Omega$. For the 6P4 SBV simulations, a d.c. circuit impedance of $1.0\ \Omega$ has been utilized; a d.c. circuit impedance of $0.0\ \Omega$ has been used for the Choudhury *et al.* HBV simulations. It is important to note that essentially identical, near-optimum embedding impedances are obtained from the harmonic-balance circuit simulator coupled to the quasi-static equivalent circuit and numerical device models for both HBVs and SBVs. Only when field-dependent electron mobility is included in the numerical device models do the near-optimum embedding impedances change significantly from the values obtained with the quasi-static device models.

The steady-state current and voltage waveforms for the 6P4 SBV doubler subject to a 100 GHz, 18.8 mW pump excitation are shown in Figure 5.30; similar waveforms for the HBV tripler subject to a 64 GHz, 20 mW pump excitation are shown in Figure 5.31. As previously noted, the relatively small differences in the results obtained from the two device modeling approaches are magnified by the nonlinearity of the device when it is embedded in a circuit. This is clearly evident from the harmonic-balance results shown in these figures. Although the current and voltage waveforms generated by the numerical and quasi-static device models have the same general shape, the sharpness, magnitudes, and phases of the waveforms differ substantially; Figure 5.30 shows even greater differences when a field-dependent electron mobility is utilized with the numerical device model.

As a result of the waveform differences shown in Figures 5.30 and 5.31, significant differences are observed in the predicted absorbed powers, output powers, and multiplying efficiencies depending on the device model utilized. In particular, predicted multiplier performance is substantially overestimated by the quasi-static equivalent circuit device/harmonic-balance circuit simulators. For the 6P4 SBV doubler, this can be seen

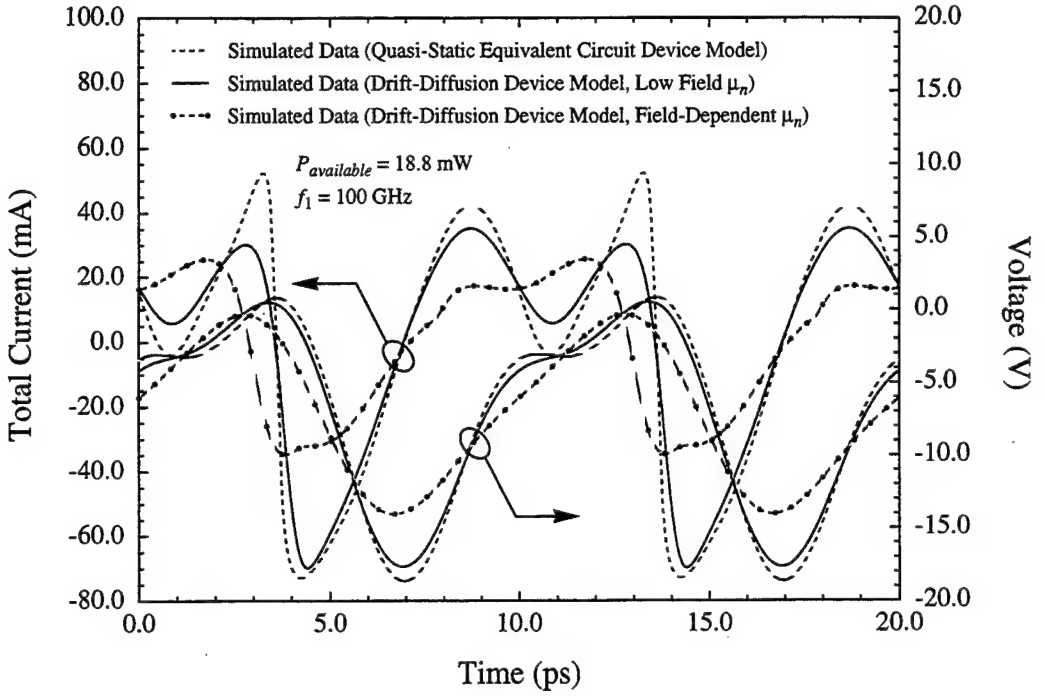

Figure 5.30 Steady-state harmonic-balance current and voltage waveforms for the UVA 6P4 GaAs SBV doubler of reference [5.6] d.c. biased at -7.03 V and subject to 100 GHz, 18.8 mW pump excitation.

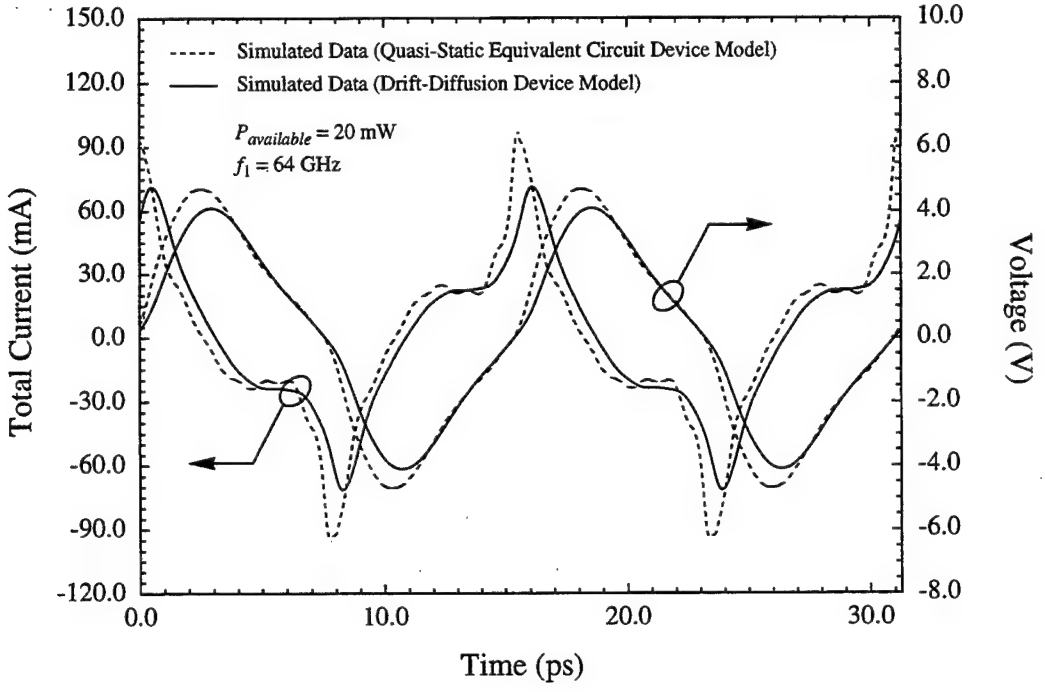

Figure 5.31 Steady-state harmonic-balance current and voltage waveforms for the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV tripler of reference [5.7] d.c. biased at 0.0 V and subject to 64 GHz, 20 mW pump excitation.

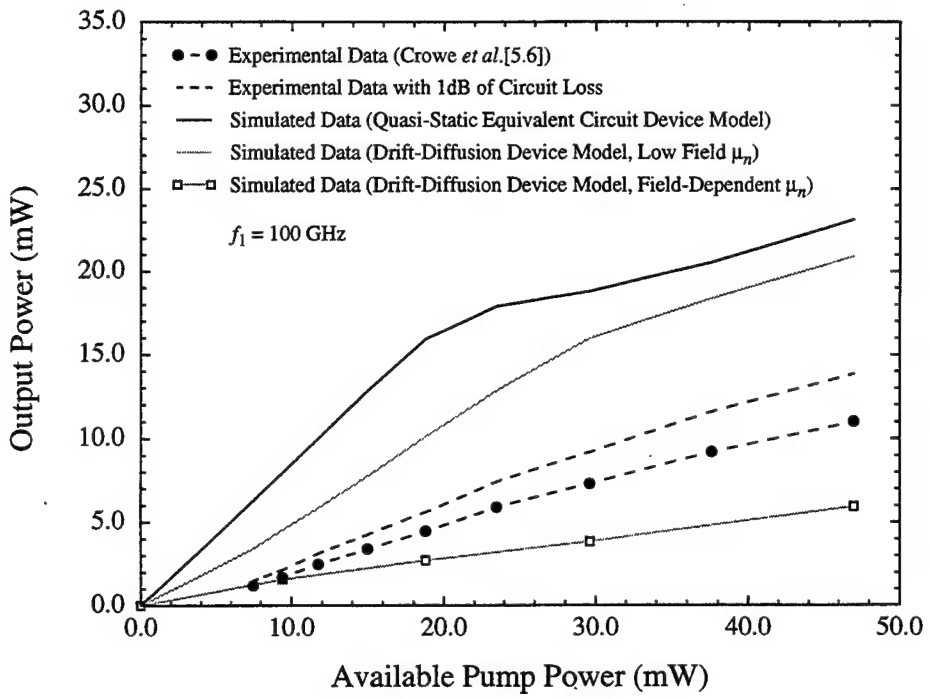

Figure 5.32 Experimental and theoretical output power versus available pump power for the UVA 6P4 GaAs SBV doubler of reference [5.6] d.c. biased as shown in Figure 5.28 and subject to 100 GHz pump excitation.

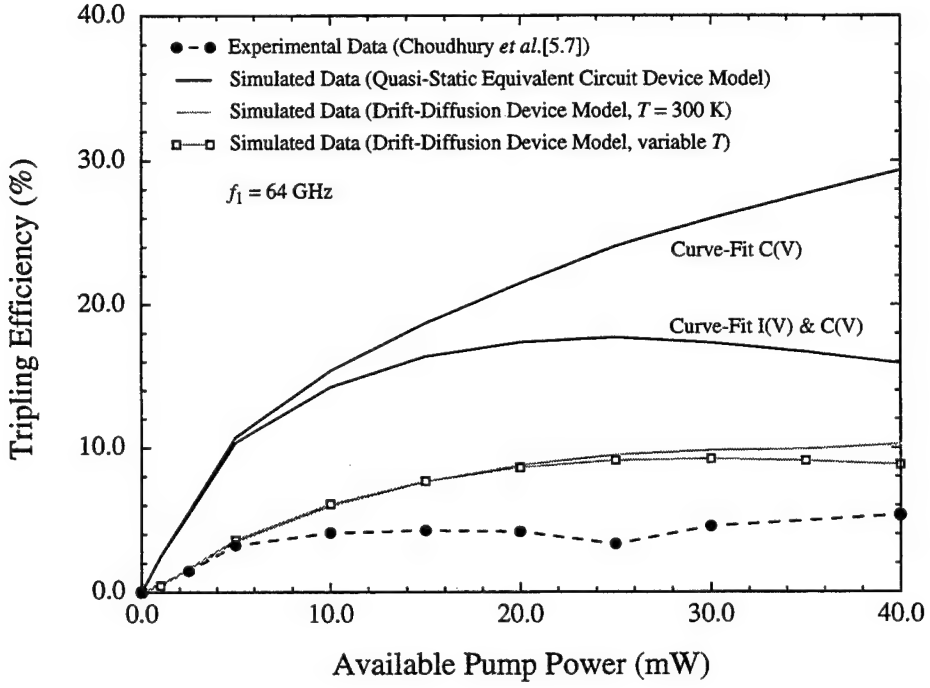

Figure 5.33 Experimental and theoretical tripling efficiency versus available pump power for the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV tripler of reference [5.7] d.c. biased at 0.0 V and subject to 64 GHz pump excitation.

clearly in Figure 5.32 which shows the experimental output power versus available pump power results for this circuit, along with the simulated results obtained from the harmonic-balance circuit simulator coupled to the two device models. Note that the experimental 6P4 SBV doubling results lie within the bounds set by the numerical device model using field-dependent and field-independent (low field) electron mobility. In particular, the experimental and field-dependent numerical device results are the same at low pump levels, but quickly diverge at higher pump levels. This result suggests that the electron mobility is drive and frequency dependent, and should be determined from large-signal sinusoidal Monte Carlo simulations rather than the usual static Monte Carlo simulations[5.20].

For the Choudhury *et al.* HBV tripler, Figure 5.33 shows the experimental tripling efficiency versus available pump power results along with results from the two simulation approaches; for simulations using the quasi-static device model, results including only the displacement current and those including both the conduction and displacement currents are shown. Also shown in Figure 5.33 is simulated data that includes thermal effects. For this particular whisker-contacted HBV tripler, the average active region temperature was estimated to be about 332 K at an available pump power of 40 mW; this temperature translates into an active region electron mobility of about 3850 $cm^2/V \cdot s$ which is about 92 percent of the 300 K mobility. Simulations including thermal effects have not been undertaken for the 6P4 SBV doubler since the average active region temperature was found to reach only about 320 K at an available pump power of 50 mW.

It is important to note that circuit losses have been accounted for in the experimental tripling efficiency data shown in Figure 5.33[5.7]; for the 6P4 SBV doubler, Figure 5.32 includes output power data assuming 1 dB of circuit loss in addition to the raw output power data. For all of the harmonic-balance simulations presented here, neither the breakdown voltage nor the critical breakdown field has been exceeded. For the 5T1 SBV doubler, however, it was found that the breakdown voltage is exceeded at relatively low available pump power levels when near-optimum circuit impedances are assumed. This suggests that careful modeling of avalanche breakdown is required to accurately simulate the performance of highly doped SBV varactors such as the 5T1 SBV doubler.

Overall, the harmonic-balance results presented here indicate that the physics-based numerical device models for SBVs and HBVs provide significantly improved correlation to experimental data when compared to typical quasi-static equivalent circuit models. The remaining discrepancies between simulation and experiment are attributed mainly to the inaccurate assumption that the multiplier circuits present optimum impedances to the active devices. The accurate determination of active device embedding impedances (for example, the impedances of waveguide mounting structures such as the one described in Chapter 7) would greatly improve the analysis and design of frequency multipliers as well as other highly nonlinear circuits. Recent work to determine the embedding impedances of SBV doubler blocks[5.21, 5.22] and Transferred Electron Oscillator (TEO) waveguide cavities[5.23] using a three-dimensional finite-element electromagnetic simulator[5.24] suggests that it is now feasible to determine these impedances for a wide range of waveguide mounting structures.

In addition to the significantly improved analysis capabilities that the numerical device/harmonic-balance circuit simulation approach affords, this approach also facilitates the careful examination of the internal physical phenomena occurring in a wide array of devices subject to actual large-signal pump excitations. Such insight is important at high frequencies and for devices, particularly novel ones such as the HBV, which are not easily modeled analytically. To illustrate this point, simulated electron concentration profiles versus time and position within a device are shown in Figures 5.34 and 5.35 for the 6P4 SBV doubler and the Choudhury *et al.* HBV tripler at 100 GHz and 64 GHz, respectively. For both multipliers, the electron concentration profiles are taken at increments of one-fiftieth of the fundamental period, or every 0.2 ps and 0.3125 ps, respectively. Note, also, that these results correspond to the field-independent harmonic-balance results shown in Figures 5.30 and 5.31, respectively.

The current saturation phenomenon discussed in *Section 5.2.1.2* can be visualized quite easily by examining the particle and displacement currents versus time and position within the 6P4 SBV doubler and the Choudhury *et al.* HBV tripler. Figures 5.36 and 5.37 show the particle and displacement currents versus time and position within the 6P4 SBV doubler at 100 GHz. Likewise, Figures 5.38 and 5.39 show the particle and displacement

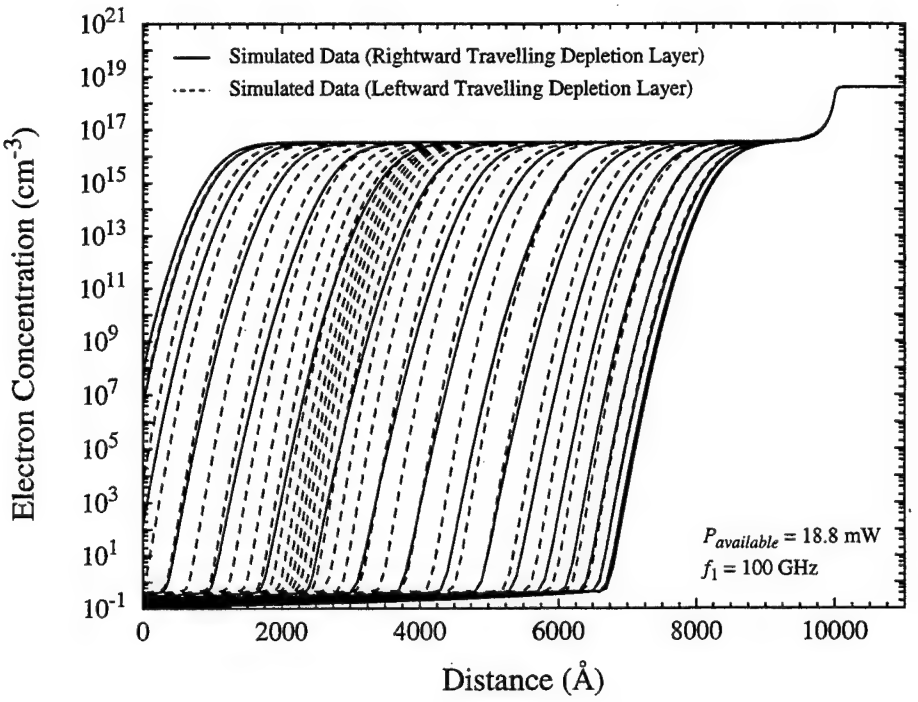

Figure 5.34 Theoretical electron concentration profiles versus time and position within the UVA 6P4 GaAs SBV doubler of reference [5.6] d.c. biased as shown in Figure 5.28 and subject to 100 GHz, 18.8 mW pump excitation.

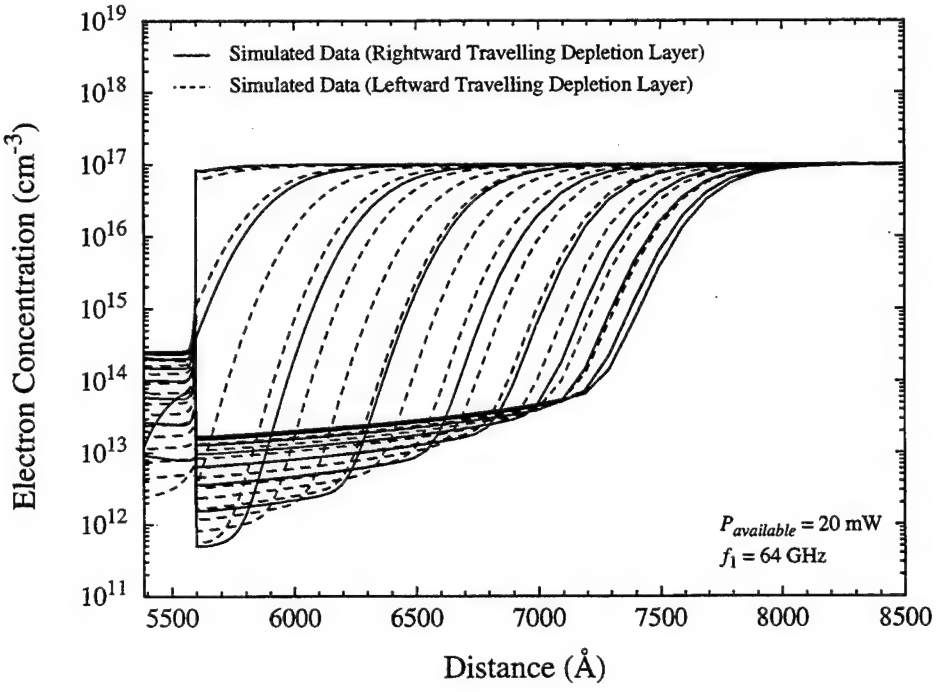

Figure 5.35 Theoretical electron concentration profiles versus time and position on the depletion side of the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV tripler of reference [5.7] d.c. biased at 0.0 V and subject to 64 GHz, 20 mW pump excitation.

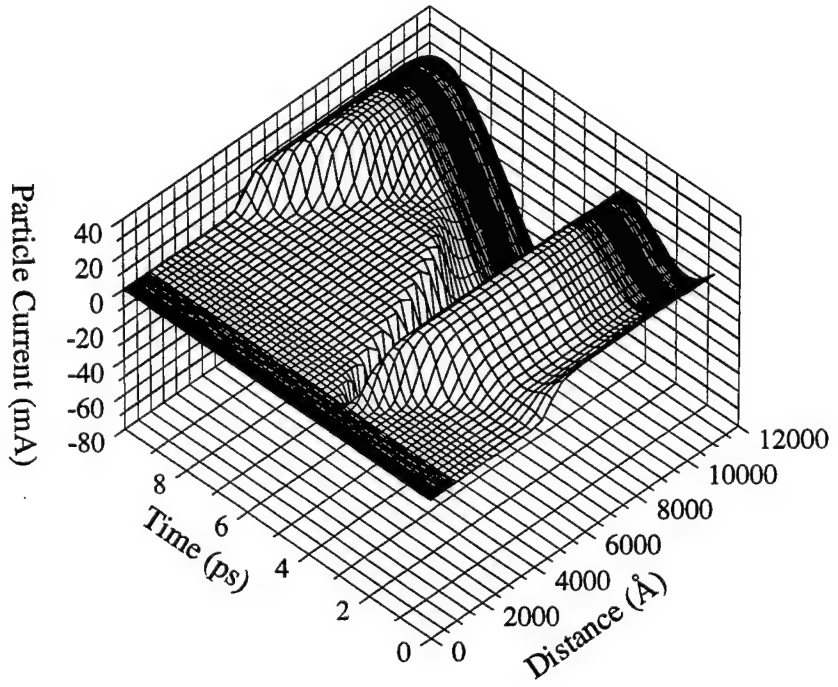

Figure 5.36 Theoretical particle current versus time and position within the UVA 6P4 GaAs SBV doubler of reference [5.6] d.c. biased as shown in Figure 5.28 and subject to 100 GHz, 18.8 mW pump excitation.

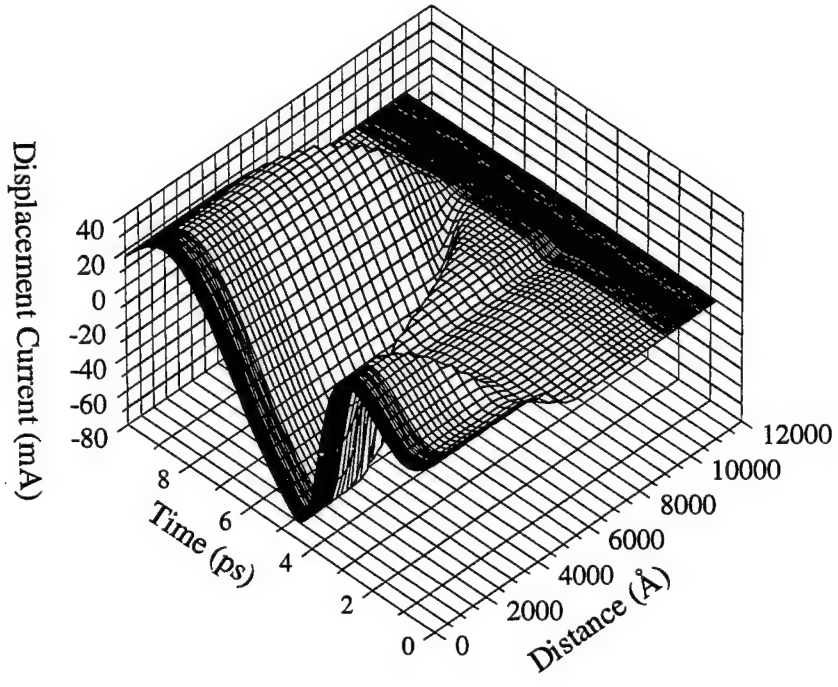

Figure 5.37 Theoretical displacement current versus time and position within the UVA 6P4 GaAs SBV doubler of reference [5.6] d.c. biased as shown in Figure 5.28 and subject to 100 GHz, 18.8 mW pump excitation.

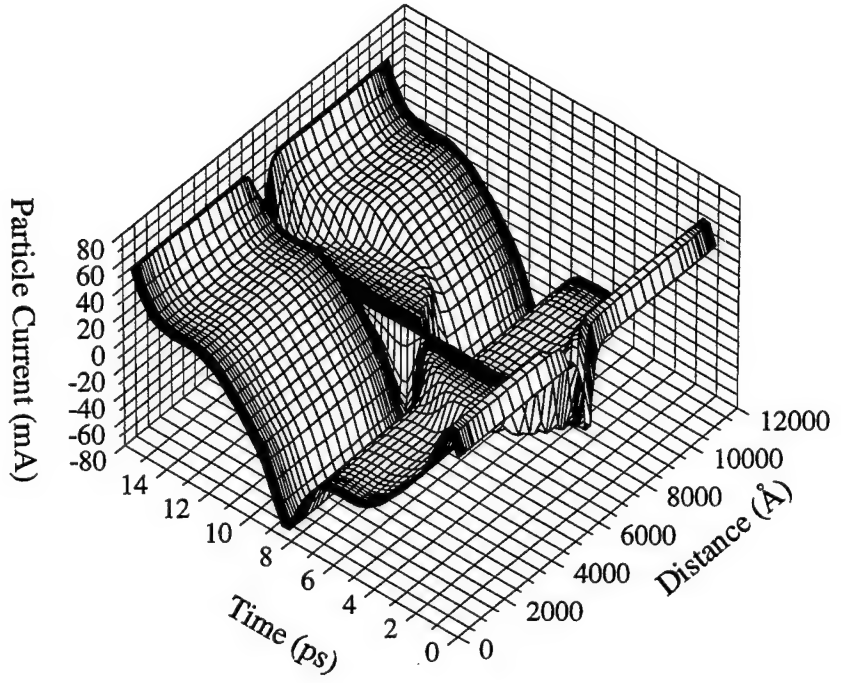

Figure 5.38 Theoretical particle current versus time and position within the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV tripler of reference [5.7] d.c. biased at 0.0 V and subject to 64 GHz, 20 mW pump excitation.

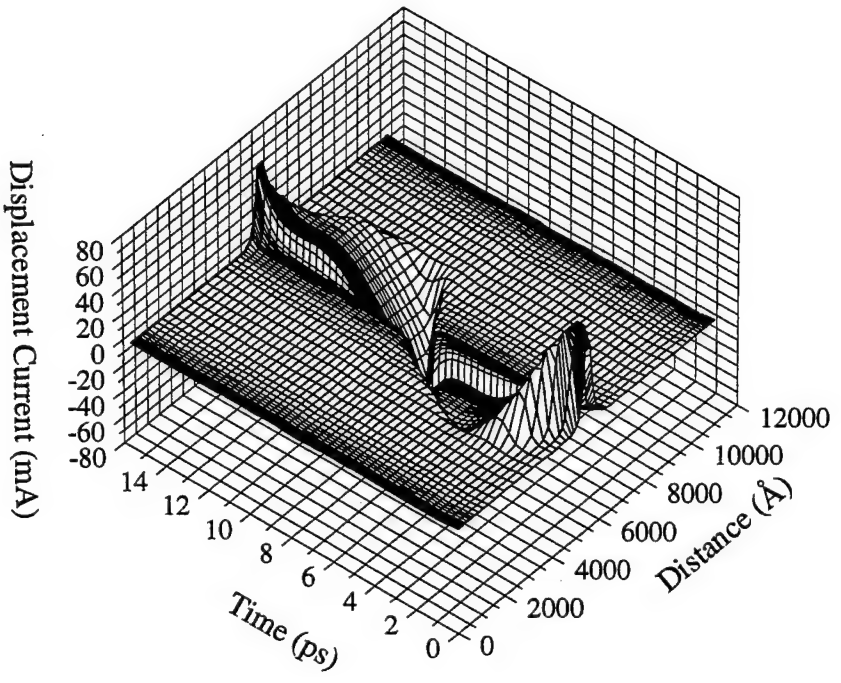

Figure 5.39 Theoretical displacement current versus time and position within the single barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV tripler of reference [5.7] d.c. biased at 0.0 V and subject to 64 GHz, 20 mW pump excitation.

currents versus time and position within the Choudhury *et al.* HBV tripler at 64 GHz. Again, note that these results correspond to the field-independent harmonic-balance results shown in Figures 5.30 and 5.31, respectively. Comparisons of the total current waveform of Figure 5.30 with the current contours of Figures 5.36 and 5.37 clearly show that the particle current in the undepleted region of the 6P4 SBV is balanced by the displacement current in the depleted region of the device such that the total current is constant at a given point in time. Similar conclusions can be drawn by comparing the total current waveform of Figure 5.31 with the current contours of Figures 5.38 and 5.39.

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Chapter 6

Heterostructure Barrier Varactor Fabrication

Heterostructure Barrier Varactor (HBV) devices were fabricated for d.c., microwave, and millimeter wave testing purposes. As noted in Chapter 5, whisker-contacted HBV devices were fabricated for d.c. tests. HBV devices embedded in coplanar waveguide were fabricated to facilitate microwave testing of HBVs using standard coplanar probing techniques. Finally, planar multi-barrier HBV devices for tripling from 80 GHz to 240 GHz were fabricated using a process in which the device "surface channel" is etched prior to formation of the contact pad-to-anode air-bridge "finger". The formation of the device air-bridge "finger" after the "surface channel" etch is facilitated by a trench planarization technique, and yields a device with minimum parasitic capacitances. An overview of the fabrication processes for whisker-contacted HBV devices and coplanar waveguide HBV test structures is given in this chapter along with a detailed description of the novel planar HBV fabrication process used to produce prototype four barrier 80/240 GHz HBV triplers.

All of the HBV material structures utilized in this work were provided by the Naval Research Laboratories (NRL). The structures were grown in a Vacuum Generators V80H Molecular Beam Epitaxy (MBE) system on (100)-oriented GaAs substrates manufactured by American Xtal Technology. The whisker-contacted HBV structures were grown on highly silicon doped ($1.4\text{-}3.0x10^{18}$ cm^{-3}) n-type substrates, while the coplanar waveguide and planar multi-barrier HBV structures were grown on semi-insulating (SI) substrates with resistivities of $5.0\text{-}7.0x10^{7}$ Ω·cm at 300 K. Both types of substrates were approximately 450 μm thick. Alloy composition and silicon doping profiles as well as layer thicknesses for the NRL-grown structures were estimated based on values extracted from calibration structures grown in the MBE system. Initial HBV material structures included epitaxial capping layers comprised of n^+ GaAs; subsequent HBV material structures

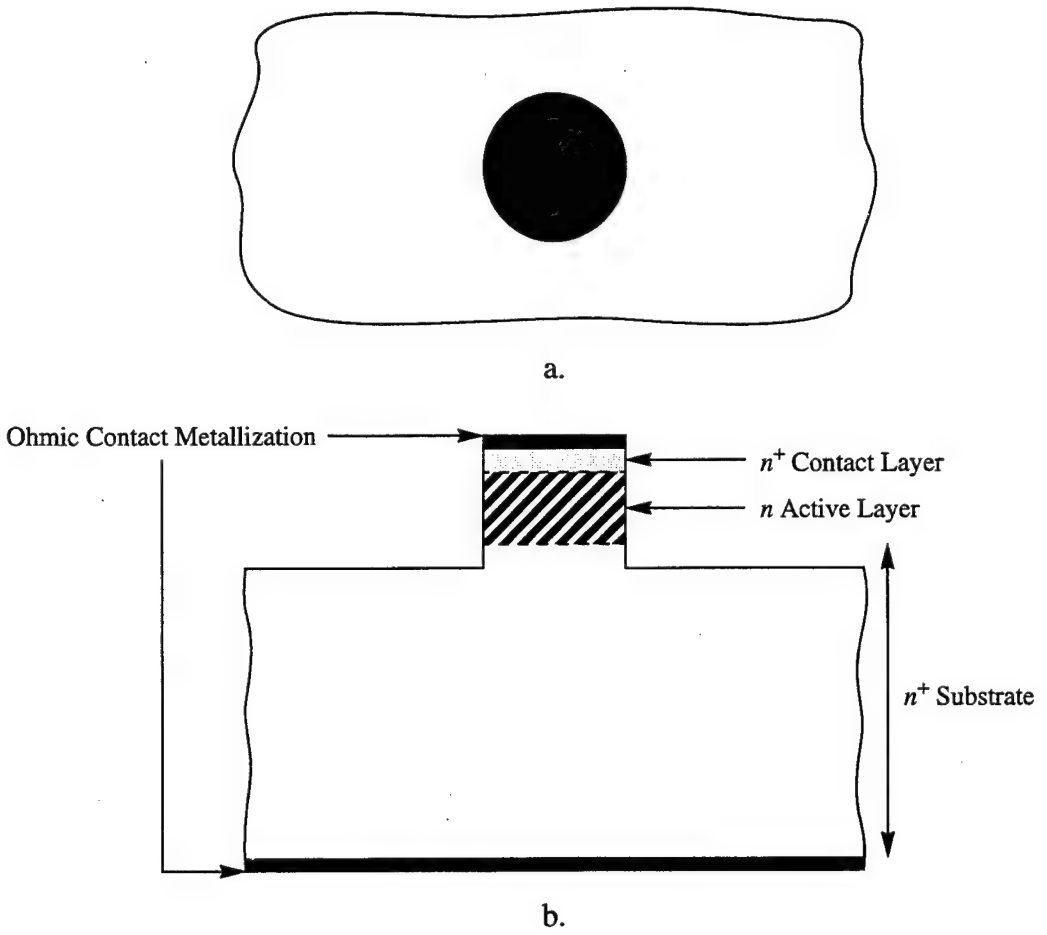


Figure 6.1 Top (a.) and cross-sectional (b.) views of the basic whisker-contacted HBV structure.

included epitaxial capping layers comprised of n^+ InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs. The epitaxial capping layers on the latter material structures were modified, based on the work of references [6.1] and [6.2], to improve the ohmic contact specific contact resistivity.

6.1 Whisker-Contacted HBVs

Arrays of circular whisker-contacted HBVs were fabricated using standard optical photolithography, metallization, and chemical etching procedures. Figure 6.1 shows top and cross-sectional views of the basic whisker-contacted HBV structure fabricated for this work. A dual-layer photoresist/electron-beam evaporation lift-off process was used to

define arrays of circular metal contacts on the n^+ epitaxial capping layer (anode contact). The individual HBV devices were then electrically isolated by reactive-ion/wet chemical etching with the metal contacts, protected by photoresist, serving as the etch mask. A 10 second wet chemical etch in 10:1:1 H_2SO_4:H_2O_2:H_2O was used to remove any damage or surface roughness introduced by the reactive-ion etch. The n^+ GaAs substrate (cathode contact) was then metallized by electron-beam evaporation, and a thick over-layer of Au was electroplated on the evaporated cathode contact metals.

Ohmic contacts were formed by alloying the anode and cathode Ni(250 Å)/Ge(325 Å)/Au(650 Å)/Ti(400 Å)/Au(2000 Å) metallization structures for 2 minutes in an alloy furnace purged with forming gas (90% N_2/10% H_2). For HBV structures having an n^+ GaAs epitaxial capping layer, the alloy temperature was approximately 400 °C; for HBV structures having an n^+ InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs epitaxial capping layer, the alloy temperature was approximately 375 °C. TLM test structures consisting of 100 μm wide by 150 μm long contact pads were fabricated on the two different HBV epitaxial structures (one having an n^+ GaAs capping layer and one having an n^+ InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs capping layer) to determine the resistance of the ohmic contacts. Average specific contact resistivities for the structures with n^+ GaAs (400 °C) and n^+ InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs (375 °C) capping layers were approximately $2.14x10^{-6}$ Ω·cm^2 and $6.82x10^{-7}$ Ω·cm^2, respectively. Overall, the Ni/Ge/Au/Ti/Au/InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs ohmic contact had a significantly lower specific contact resistivity than the Ni/Ge/Au/Ti/Au/GaAs ohmic contact. In addition, the morphology of the alloyed Ni/Ge/Au/Ti/Au/InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs contact was significantly smoother than that of the alloyed Ni/Ge/Au/Ti/Au/GaAs contact since it was alloyed at a lower temperature.

6.2 Coplanar Waveguide HBV Test Structures

Coplanar waveguide HBV test structures (HBV devices embedded in coplanar waveguide) were fabricated using standard optical photolithography, metallization, and chemical etching procedures. Identical coplanar waveguide test structures with

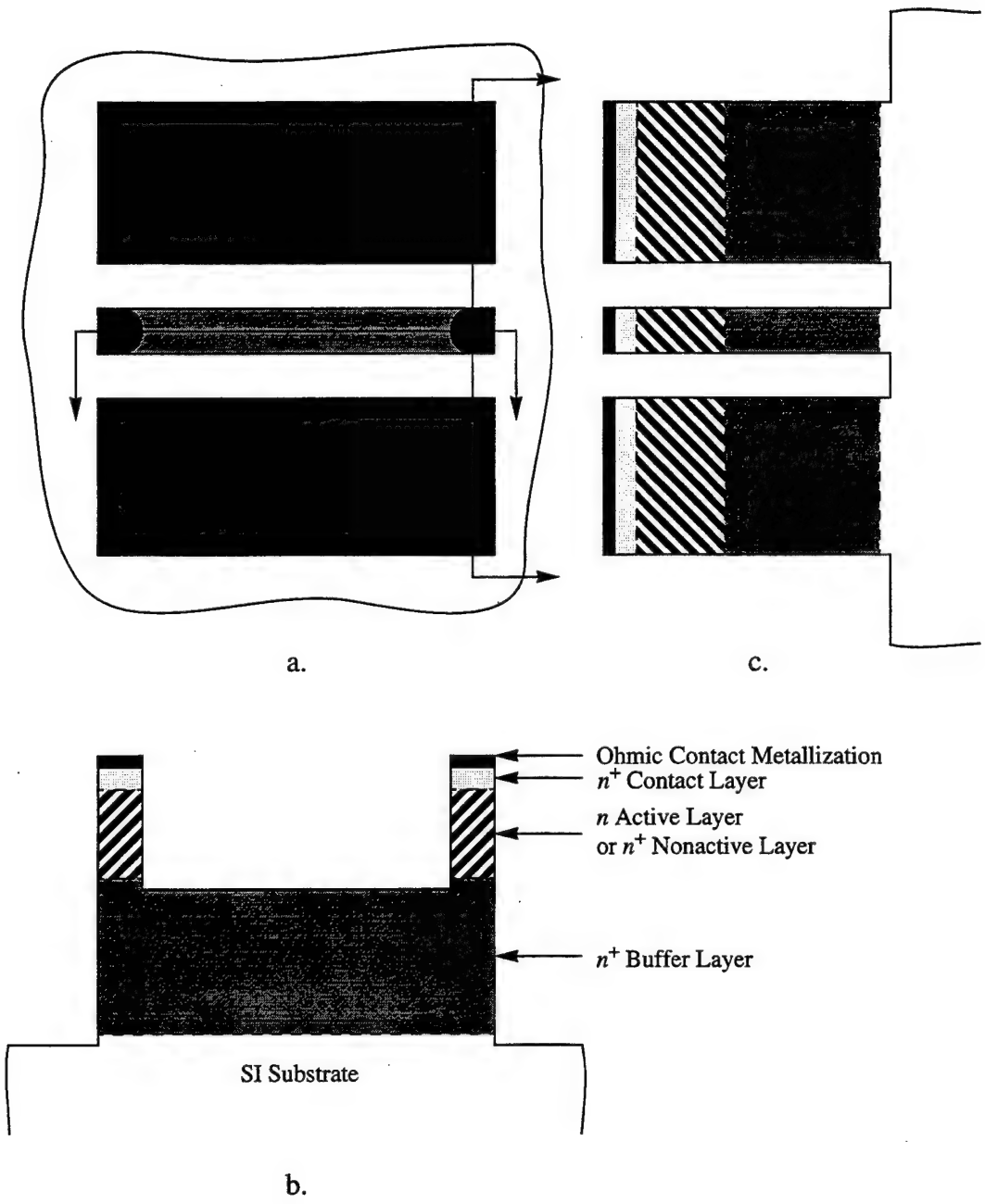


Figure 6.2 Top (a.) and cross-sectional (b. and c.) views of a two-port (transmission/reflection) coplanar waveguide test structure.

n^+ nonactive layers replacing the n active layers were also fabricated for use in determining the parasitic elements of the coplanar waveguide test structures. Figure 6.2 shows top and cross-sectional views of the basic two-port (transmission and reflection) coplanar waveguide structures fabricated for this work. The ground planes for all of the structures

were 225 μm wide and spaced 50 μm from the 75 μm diameter device anodes; the separation between the device anodes varied from 25 μm to 225 μm. As with the whisker-contacted HBVs, a dual-layer photoresist/electron-beam evaporation lift-off process was used to define anode and ground plane metal contacts on the n^+ epitaxial capping layer. The individual device mesas were then electrically isolated using a reactive-ion/wet chemical etch process. During this process, the semiconductor material was reactive-ion etched down to the n^+ buffer layer with the metal contacts, protected by photoresist, serving as the etch mask. The semiconductor material was then reactive-ion etched down to the SI substrate with the metal contacts and the n^+ semiconductor strip connecting the anodes, protected by photoresist, serving as the etch mask. A 10 second wet chemical etch in 10:1:1 H_2SO_4:H_2O_2:H_2O was then used to remove any damage or surface roughness introduced by the reactive-ion etch. Ohmic contacts were formed by alloying the Ni(250 Å)/Ge(325 Å)/Au(650 Å)/Ti(400 Å)/Au(2000 Å) metallization structures for 2 minutes in an alloy furnace purged with forming gas (90% N_2/10% H_2). Again, for structures having an n^+ GaAs epitaxial capping layer, the alloy temperature was approximately 400 °C; for structures having an n^+ InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$/GaAs epitaxial capping layer, the alloy temperature was approximately 375 °C.

6.3 Planar Multi-Barrier HBVs for High Frequency Tripling

6.3.1 Planar HBV Fabrication Process Overview

Unlike the Schottky Barrier Varactor (SBV) where the cross-sectional area controlling charge modulation is defined by the area of the anode, the cross-sectional area controlling charge modulation in an HBV is defined by the cross-sectional areas of both the barrier and modulation regions of the device. As a result, the fabrication of planar HBVs requires either an ion implant isolation step or a mesa-isolation etch step to define the active region of the device. In the present work, planar mesa-isolated HBVs have been produced using a fabrication procedure in which the device "surface channel" is etched prior to formation of the contact pad-to-anode air-bridge "finger"[6.3]. Formation of the device air-bridge "finger" after etching the "surface channel" is facilitated by using the trench

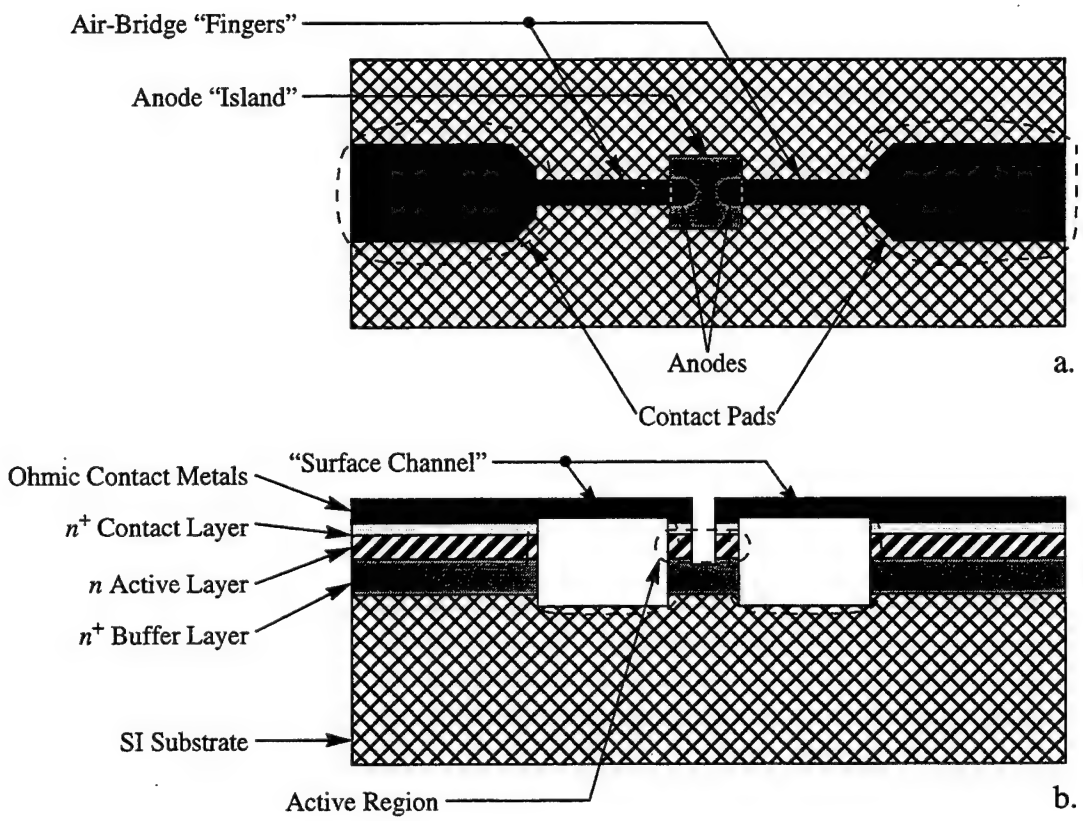


Figure 6.3 Top (a.) and cross-sectional (b.) views of the planar HBV device layout.

planarization technique of reference [6.3], and yields a device with minimal parasitic capacitances since the fringing capacitances between the device active region "mesa" and the air-bridge "finger" are minimized. The basic concept underlying this planarization technique was first proposed by Dill[6.4].

Although the present focus is on HBVs, the "surface channel" etch/epoxy planarization/"finger" electroplating process is applicable to a wide variety of planar devices. As suggested in reference [6.3], for example, the performance of the University of Virginia (UVA) "surface channel" Schottky diode[6.5, 6.6] would be improved greatly if its fabrication procedure were modified to accommodate the "surface channel"/epoxy planarization/"finger" electroplating process.

The basic planar HBV device layout used in this work is shown in Figure 6.3. This back-to-back layout yields an inherently multi-barrier device; it has been utilized here to

compensate for any asymmetry in the MBE-grown epitaxial structure and to double the number of barriers obtained from a given HBV epitaxial structure. The general planar HBV fabrication process developed for this work is outlined schematically in Figure 6.4. An overview of this process is given, in reference to Figure 6.4, below:

a. Deposit Ni(250 Å)/Ge(325 Å)/Au(650 Å)/Ti(400 Å)/Au(2000 Å) ohmic contact metallization in device anode and contact pad regions using a dual-layer photoresist/electron-beam evaporation lift-off process, and alloy ohmic contacts in a forming gas ambient (90% N_2/10% H_2) for 2 minutes.

b. Form device "surface channel" to isolate anode and contact pad regions using a photoresist protection/reactive-ion etch process.

c. Planarize device "surface channel" using a low viscosity thermosetting epoxy and a planarizing superstrate as shown in Figure 6.5. The bulk epoxy planarization process used here was developed by Bill Bishop at UVA.

d. After exposing the device contact pads and anodes by O_2 plasma etching the epoxy, spin a very thin layer of photoresist on the wafer to improve the uniformity of the bulk epoxy planarization step, and redefine the device contact pads and anodes in the photoresist[6.7, 6.8].

e. Sputter deposit Cr/Au "seed" metallization on entire wafer, pattern contact pad-to-anode air-bridge "finger" structures in photoresist, and d.c. electroplate the entire contact pad/air-bridge "finger"/anode structures.

f. Remove epoxy/photoresist planarization material using an O_2 plasma etch process[6.7, 6.8].

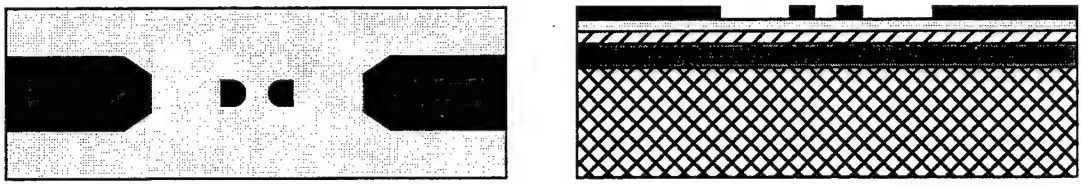
g. Isolate device anodes using a photoresist protection/reactive-ion etch process.

The fabrication process is completed by making dice cuts at the boundaries of the individual chips while protecting the frontside of the wafer with a polymer protective coating, and lapping the backside of the wafer in order to thin the wafer and separate the individual chips.

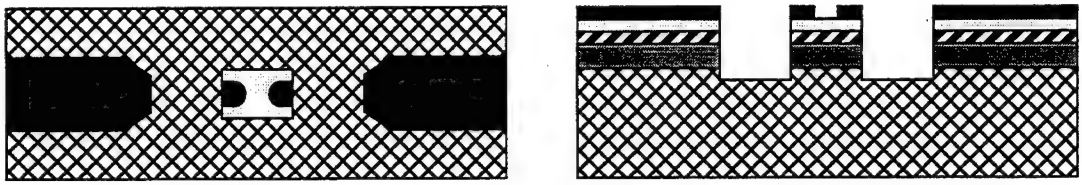
6.3.2 Fabrication of Prototype Four Barrier GaAs/AlGaAs HBVs

Prototype planar four barrier HBVs for tripling from 80 GHz to 240 GHz were produced using the fabrication process outlined in *Section 6.3.1*. The MBE-grown epitaxial structure for the prototype HBVs is given in Table 6.1. A given photolithographic level on

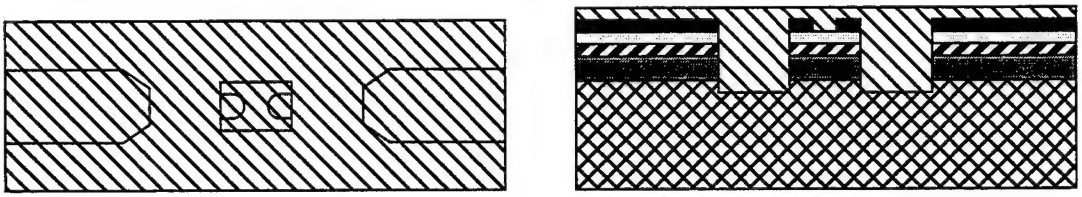
a. Metallization of device anode and contact pad ohmic contacts



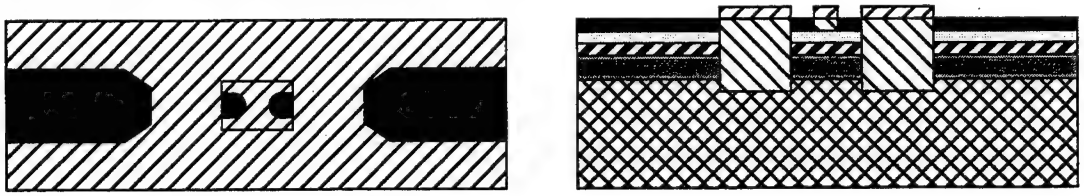
b. Reactive-ion etch of device "surface channel"



c. Bulk (epoxy) planarization of device "surface channel"



d. Final (photoresist) planarization of device "surface channel"



e. Electroplating of Au device air-bridge "fingers"

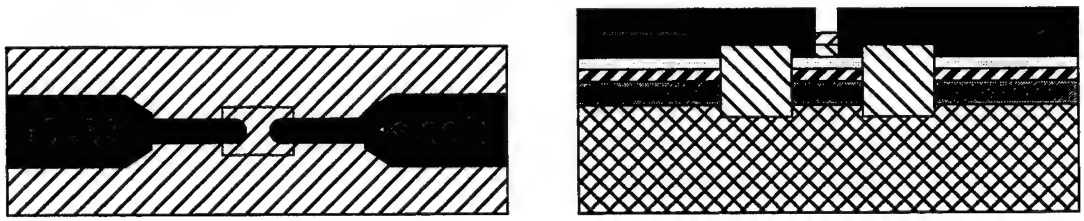
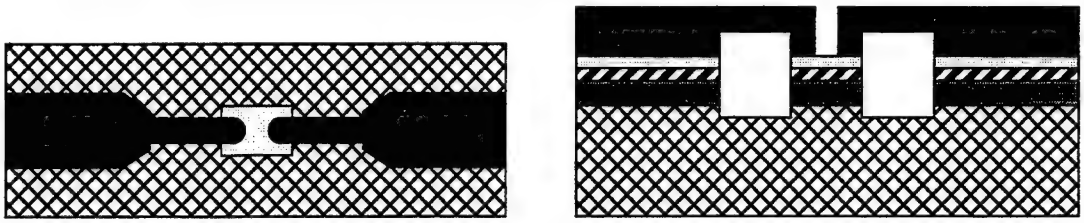


Figure 6.4 Top and cross-sectional views of the fabrication steps for the fabrication of planar HBVs.

f. Removal of epoxy/photoresist planarization material



g. Reactive-ion etch to isolate device anodes

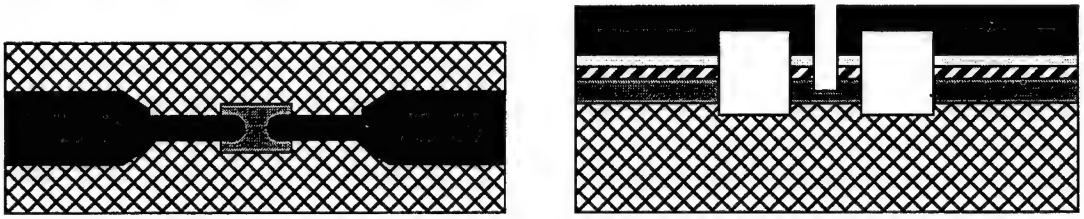


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Figure 6.4, continued.

the mask used to fabricate these devices contained of an array of devices with 6 μm (3 μm), 8 μm (3 μm, 4 μm, and 5 μm), and 10 μm (4 μm) anode diameters ("finger" widths). For all devices, the contact pads were 30 μm wide and 60 μm long, while the "fingers" were 50 μm long and the anodes were spaced 5 μm apart. Figure 6.6 shows a scanning electron micrograph of a completed prototype four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV having 8 μm diameter anodes, 4 μm wide "fingers", and a total chip thickness of approximately 2.25 mils. A close-up view of the device anode "island" is shown in Figure 6.7. The etch depth for the device "surface channel" is approximately 10 μm, while the height of the anode "mesas" is approximately 3 μm. The actual anode diameter is approximately 8.75 μm since a 1.5 minute 10:1 50 % citric acid:H_2O_2 wet chemical etch was used to

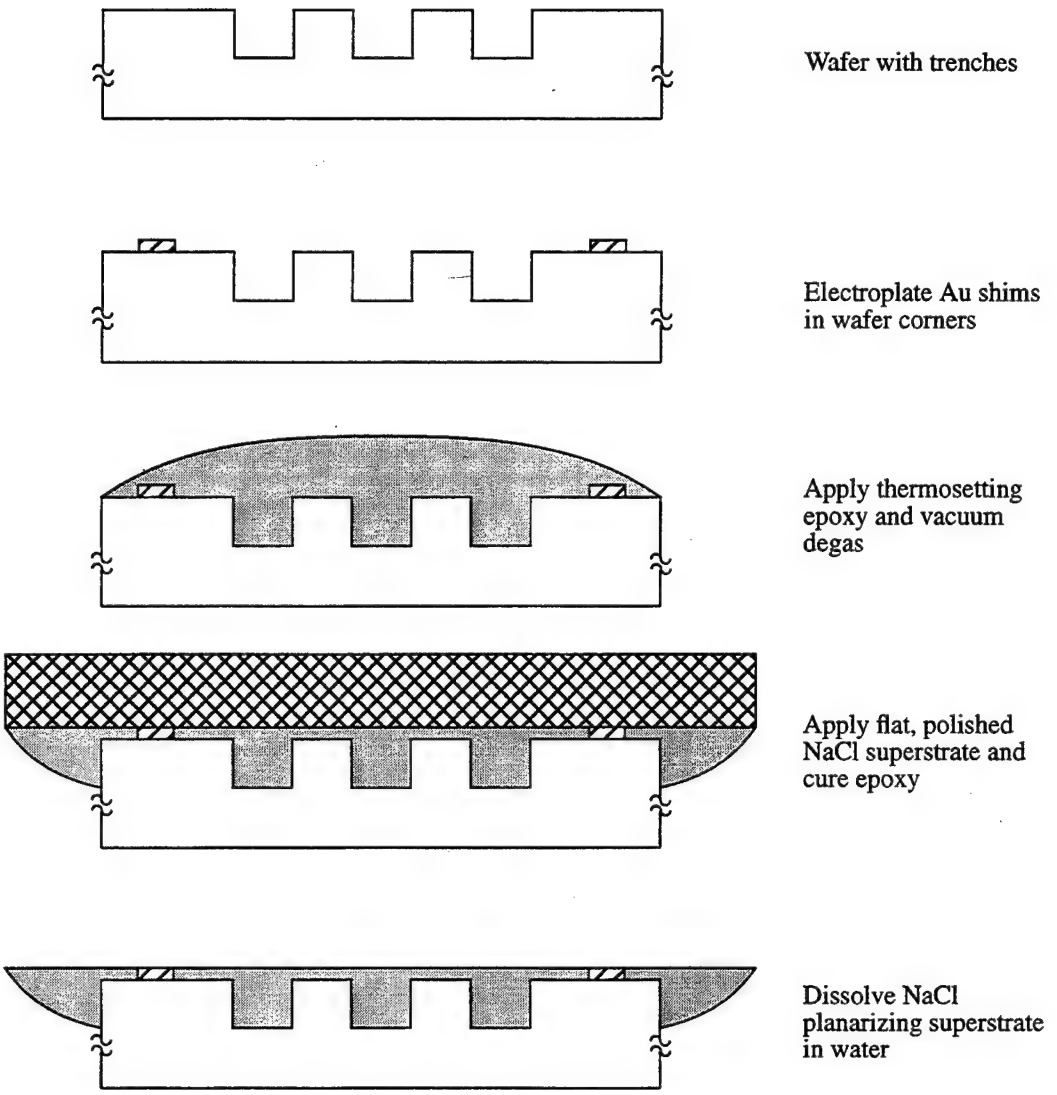

Figure 6.5 Superstrate Replica Planarization process of reference [6.3] used in the present work.

improve the quality of the "mesa" sidewalls and the anode isolation region following the device anode reactive-ion isolation etch.

It is important to note that the prototype devices have a partial rim of active region conductive material around the device anode "islands" (see Figure 6.7). This rim does not affect the electrical performance of the prototype devices, however, since it is not continuous (it does not provide a short between the two anodes). The rim is an artifact of the fabrication process used to make the prototype devices. In particular, the epoxy

Table 6.1 UVA-NRL-1174 two barrier GaAs/AlGaAs HBV material structure.

	Layer Thickness	Layer Doping	Material
n^+ Contact Layer	100 Å	n^+	InAs
	400 Å	n^+	$In_{1.0-0.0}Ga_{0.0-1.0}As$
	3000 Å	n^+	GaAs
n Active Layer	2500 Å	n ($8x10^{16}$ cm^{-3})	GaAs
	35 Å	i	GaAs
	200 Å	i	$Al_{0.7}Ga_{0.3}As$
	35 Å	i	GaAs
	5000 Å	n ($8x10^{16}$ cm^{-3})	GaAs
	35 Å	i	GaAs
	200 Å	i	$Al_{0.7}Ga_{0.3}As$
	35 Å	i	GaAs
	2500 Å	n ($8x10^{16}$ cm^{-3})	GaAs
n^+ Buffer Layer	4 μm	n^+	GaAs
Substrate	450 μm	SI	GaAs

planarization layer partially protected this rim of active region material during the anode isolation reactive-ion etch step because the side walls of the anode "island" were not perfectly vertical (the area of the anode "island" increases slightly with "surface channel" etch depth). To alleviate this problem, it is recommended that the epoxy around the device anode "island" be removed prior to the anode isolation reactive-ion etch, regardless of the quality (verticality) of the "surface channel" side walls. Furthermore, it is suggested that an Ar sputter etch be used prior to the "surface channel" and anode isolation reactive-ion etches to remove the InAs/$In_{1.0-0.0}Ga_{0.0-1.0}As$ epitaxial capping layer and, thus, improve the quality of the reactive-ion etches - it is thought that the presence of this epitaxial capping layer degrades the quality of the current low temperature reactive-ion etch process as a direct consequence of the high indium concentration of this layer and the low desorption rate of indium compounds in the presence of chlorine-based etch compounds[6.9].

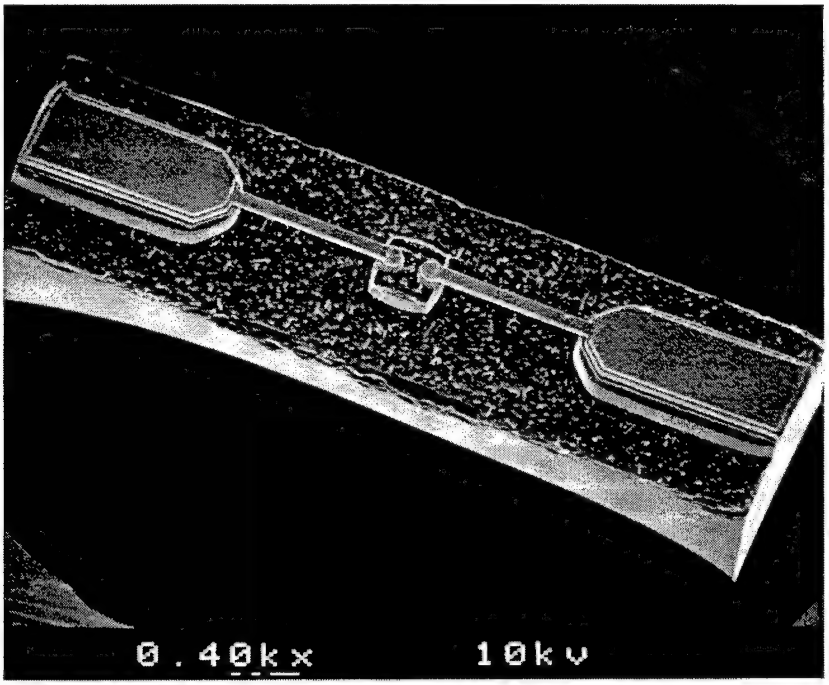

Figure 6.6 Scanning electron micrograph of a planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV chip (UVA-NRL-1174-K). The anodes are 8 μm in diameter, and the "fingers" are 4 μm wide.

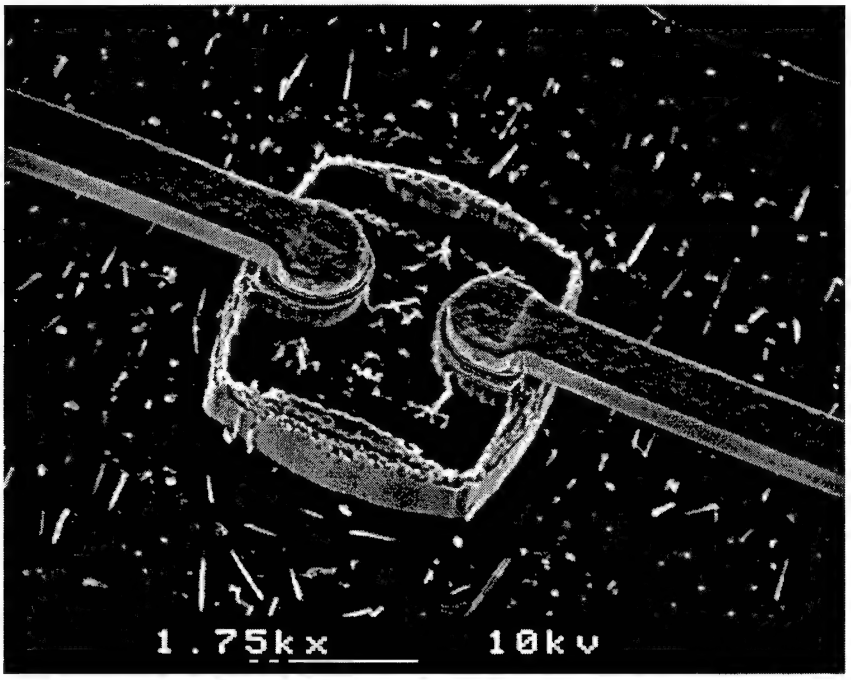

Figure 6.7 Scanning electron micrograph of the anode "island" of the planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV chip (UVA-NRL-1174-K) of Figure 6.6. The device active region "mesas" are visible under the enlarged ends of the device "fingers".

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Chapter 7

Heterostructure Barrier Varactor Experimental Test Results

7.1 D.C. Current-Voltage and Static Capacitance-Voltage Results

The planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ Heterostructure Barrier Varactor (HBV) devices and coplanar waveguide HBV test structures of Chapter 6 were analyzed to determine their d.c. current-voltage (I-V) and static capacitance-voltage (C-V) characteristics. The d.c. I-V characteristics were measured using a Hewlett-Packard (HP) 4145B semiconductor parameter analyzer. The static C-V characteristics were measured using an HP 4275A multi-frequency LCR meter with a local oscillator voltage between 0.01 V and 0.04 V, and an excitation frequency of 4 MHz; the devices were biased using a Keithley 238 high current source measure unit. Figure 7.1 shows the experimental d.c. I-V and static C-V characteristics of the UVA-NRL-1174-K planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBVs with nominal 10 μm diameter anodes; a series impedance of 4.9 Ω has been estimated for these devices. Likewise, Figure 7.2 shows the experimental and simulated d.c. I-V and static C-V characteristics of coplanar waveguide HBV test structures comprised of the same material as the planar four barrier HBVs.

7.2 Coplanar Waveguide S-Parameter Results

Two-port s-parameter measurements were made on the coplanar waveguide HBV test structures described in Chapter 6 at frequencies between 45 MHz and 25 GHz. The measurement setup used in this work consisted of a Karl Suss PM5 analytical probe station with PicoProbe 67-A-GSG-150P coplanar probes[7.1] connected via semi-rigid coaxial cable to an HP 8510C network analyzer having an HP 8517A s-parameter test set (45 MHz-50 GHz) and an HP 83165A synthesized sweeper (45 MHz-50 GHz). The network analyzer and coplanar probes were calibrated via a two-port open/short/load/through calibration procedure. The calibration standards were provided by

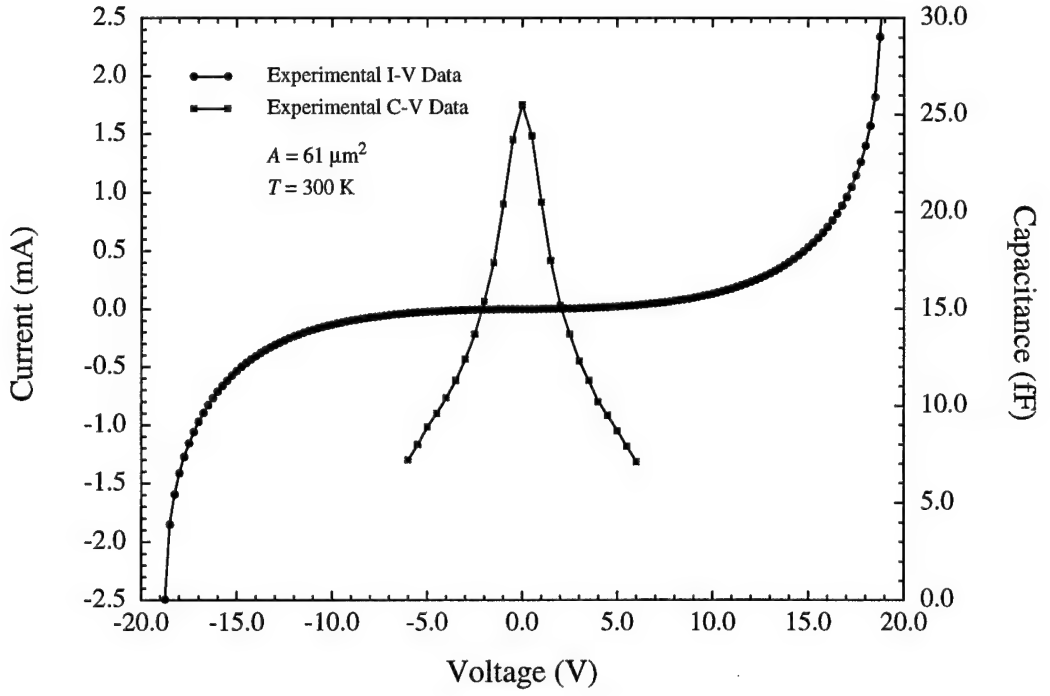


Figure 7.1 Experimental d.c. I-V and static C-V characteristics for UVA-NRL-1174-K 8.75 μm diameter, planar four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBVs.

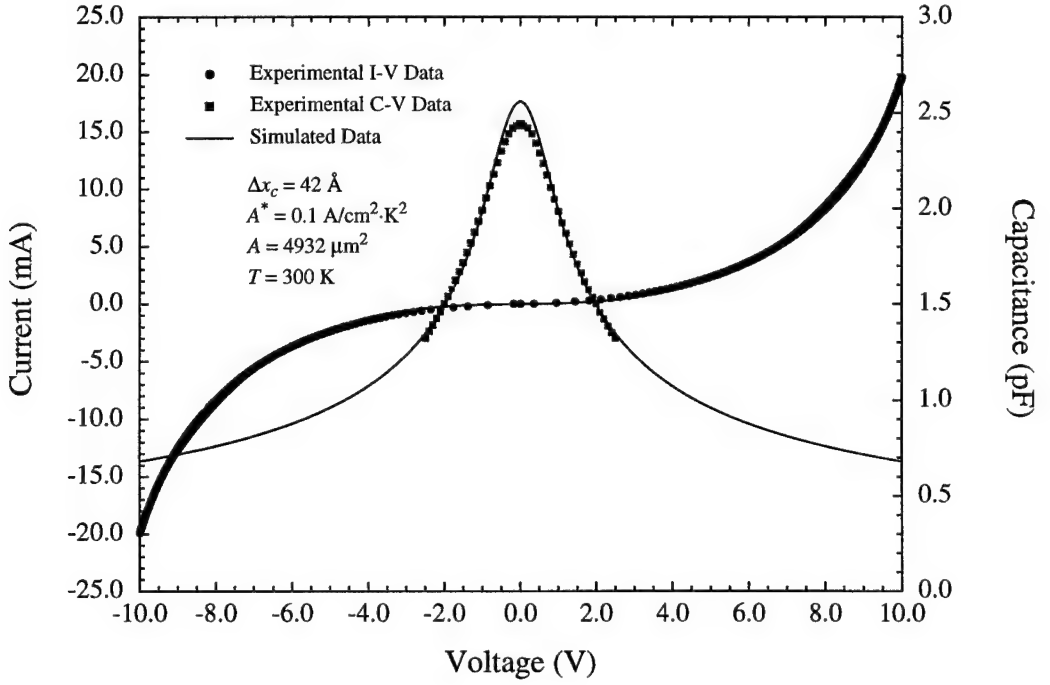


Figure 7.2 Experimental and theoretical d.c. I-V and static C-V characteristics for UVA-NRL-1174-F 75 μm diameter, coplanar waveguide four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV test structures.

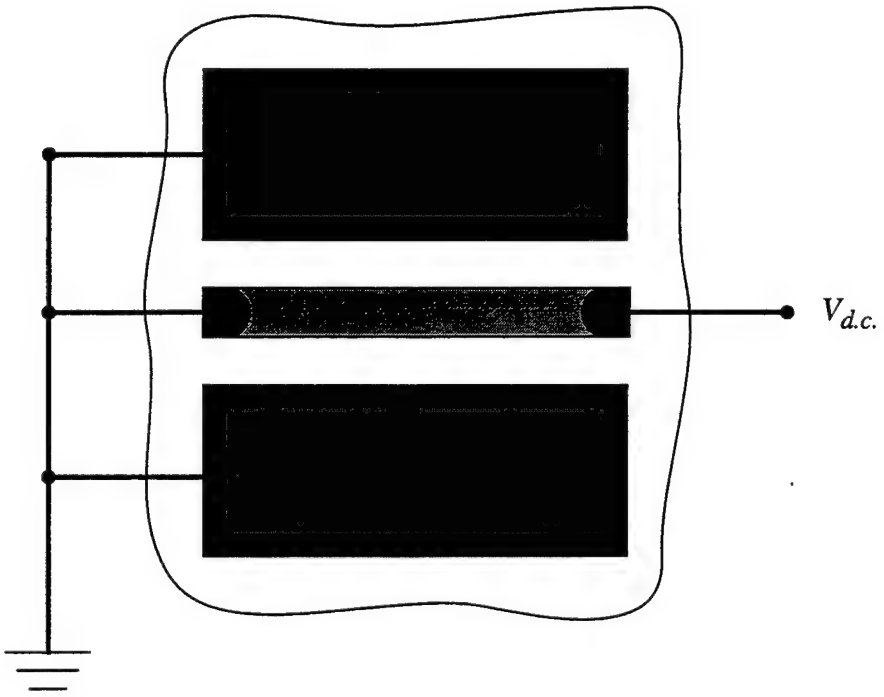


Figure 7.3 Coplanar waveguide HBV test structure d.c. bias configuration.

the manufacturer of the coplanar probes on an alumina calibration substrate (Model CS-5). The HBV test structures were biased, as shown in Figure 7.3, using a Keithley 230 programmable voltage source connected to the test set of the network analyzer. The r.f. power level used during the measurements ranged from approximately -17 dBm at 45 MHz to approximately -31 dBm at 25 GHz, and were low enough to evaluate the small-signal properties of the HBV test structures.

Figures 7.4-7.8 show the measured two-port s-parameters from 45 MHz to 25 GHz for the UVA-NRL-1174-F 75 μm diameter coplanar waveguide four barrier $GaAs/Al_{0.7}Ga_{0.3}As$ HBV test structures biased, as shown in Figure 7.3, at 0.0 V, 5.0 V, 10.0 V, -5.0 V, and -10.0 V. For all five graphs, the reflection coefficients (S_{11} and S_{22}) are predominantly in the lower half of the Smith chart while the transmission coefficients (S_{21} and S_{12}) are in the upper half of the Smith chart. As expected for the symmetric HBV structure, the measured s-parameters are symmetric with respect to port number and bias polarity. Overall, it should be possible to extract the bias-dependent parameters of an equivalent circuit model from measured s-parameters such as those shown in

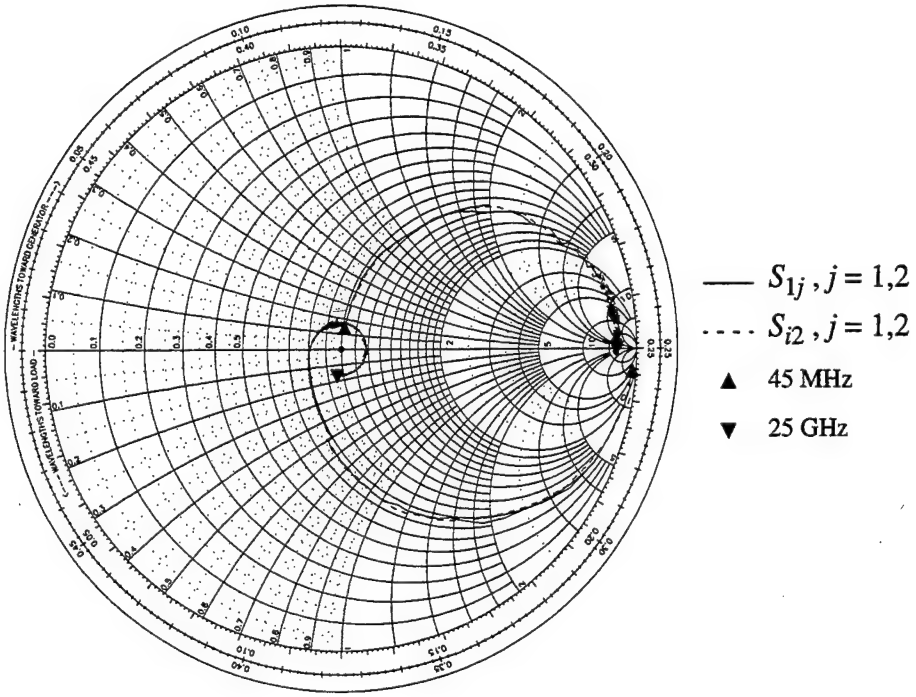


Figure 7.4 Experimental s-parameters for UVA-NRL-1174-F 75 μm diameter, coplanar waveguide four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV test structures biased, as shown in Figure 7.3, at 0.0 V.

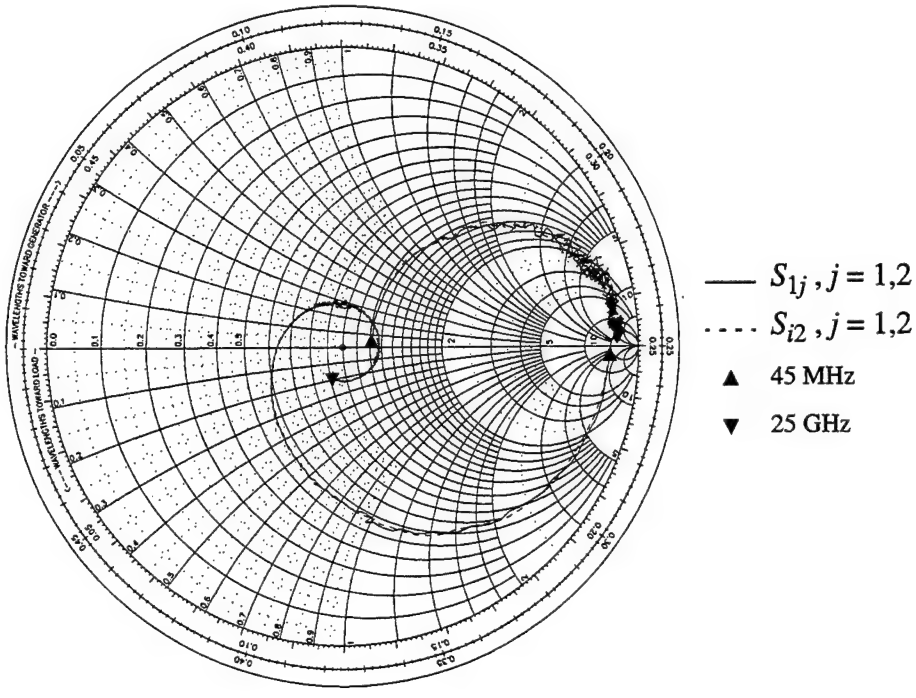


Figure 7.5 Experimental s-parameters for UVA-NRL-1174-F 75 μm diameter, coplanar waveguide four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV test structures biased, as shown in Figure 7.3, at 5.0 V.

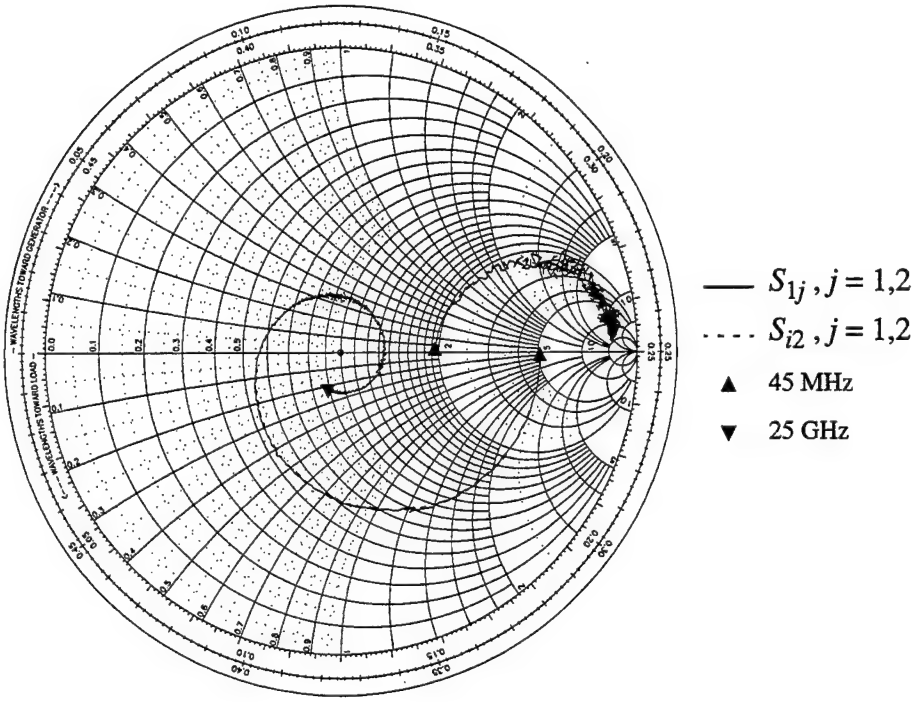


Figure 7.6 Experimental s-parameters for UVA-NRL-1174-F 75 µm diameter, coplanar waveguide four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV test structures biased, as shown in Figure 7.3, at 10.0 V.

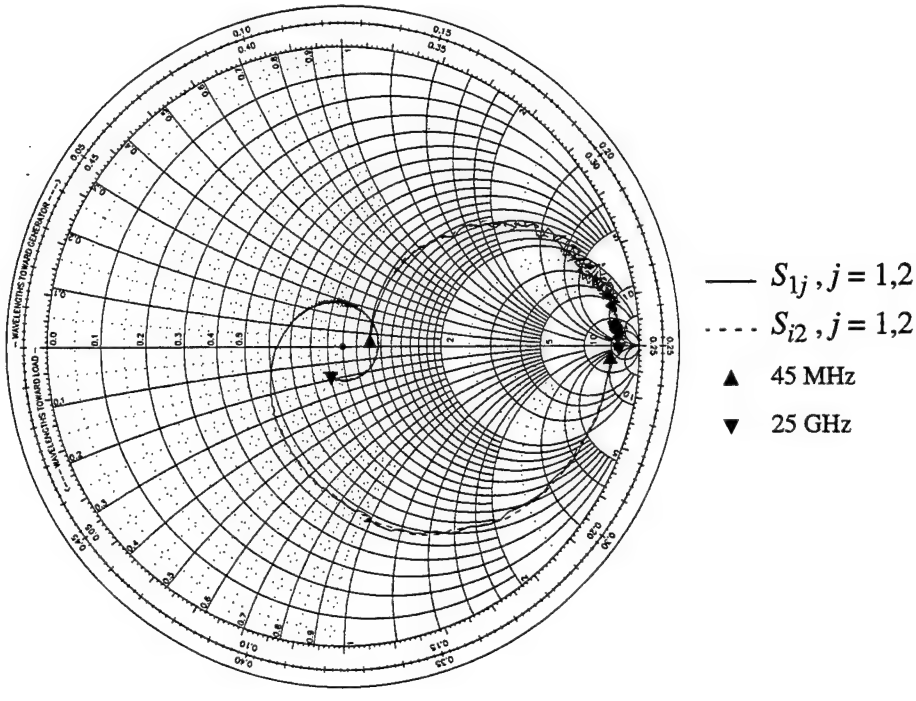


Figure 7.7 Experimental s-parameters for UVA-NRL-1174-F 75 µm diameter, coplanar waveguide four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV test structures biased, as shown in Figure 7.3, at -5.0 V.

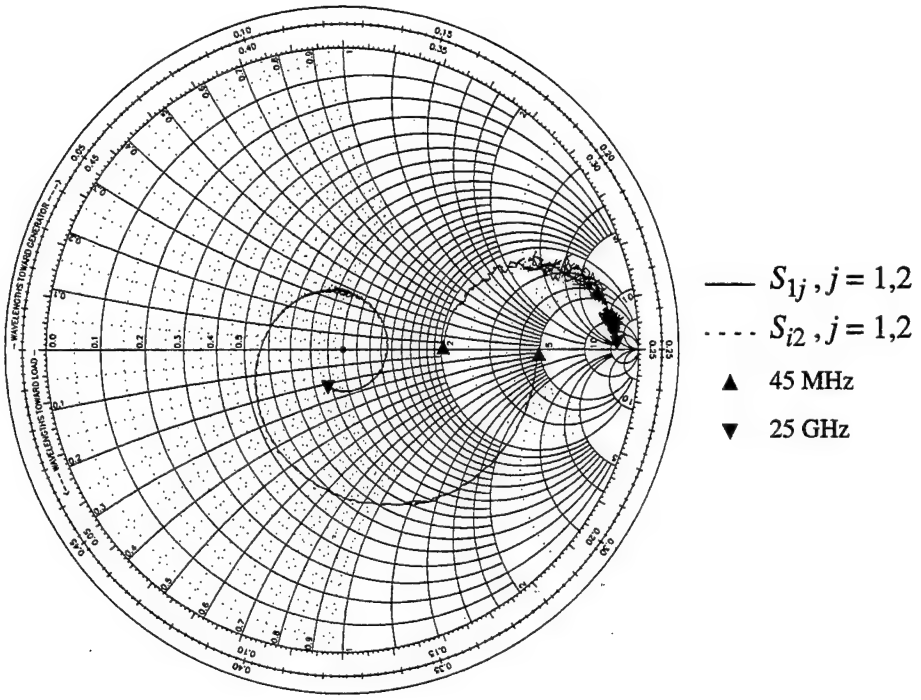


Figure 7.8 Experimental s-parameters for UVA-NRL-1174-F 75 μm diameter, coplanar waveguide four barrier *n* GaAs/*i* GaAs/*i* $Al_{0.7}Ga_{0.3}As$ HBV test structures biased, as shown in Figure 7.3, at -10.0 V.

Figures 7.4-7.8. Such information can aid in verifying the capacitance modulation of varactors, particularly ones with non-negligible conduction current such as the GaAs/AlGaAs HBV.

7.3 80/240 GHz Tripler Results

7.3.1 80/240 GHz Tripler Block

The tripler block used in this work was a National Radio Astronomy Observatory (NRAO) block (A2621-TR2-T12) designed for use in the 200-290 GHz output frequency range[7.2]. The block employs split-block construction with the input and output waveguides perpendicular to one another, and was originally designed for use with University of Virginia (UVA) 5M2 whisker-contacted Schottky Barrier Varactors (SBVs) having 5 μm diameter anodes and active region doping levels of $3.5x10^{16}$ cm^{-3}. Figure 7.9 shows the two halves of the unassembled block while Figure 7.10 shows the block fully

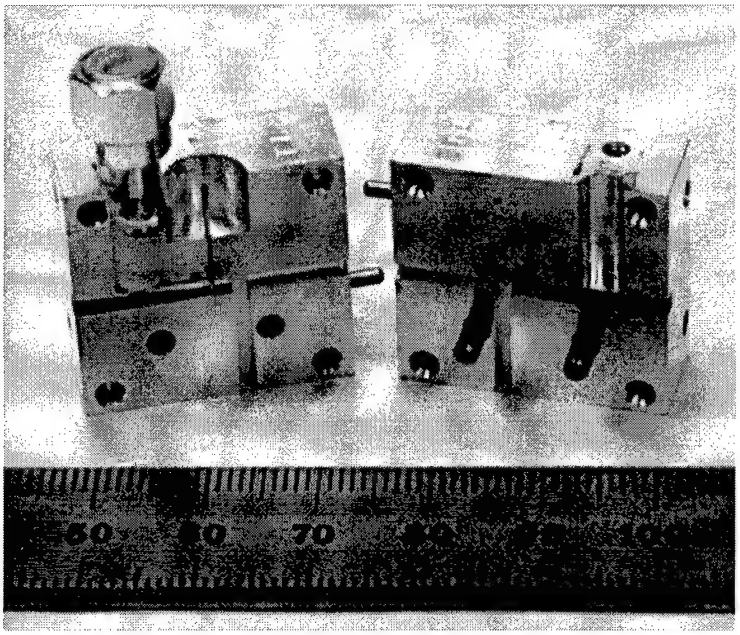


Figure 7.9 The two halves of the unassembled NRAO A2621-TR2-T12 200-290 GHz tripler block. The input waveguide is the horizontal channel in the center of each half of the block. The input waveguide probe can be seen extending into this channel in the center of the left-hand half of the block, while the output waveguide can be seen in the center of the right-hand half of the block.

assembled. Using UVA 5M2 and UVA 6P4 whisker-contacted SBV diodes, this tripler block provides more than 2 mW of power across the entire 200-290 GHz output band[7.2].

Figure 7.11 is a detailed schematic diagram of the internal configuration of the tripler block utilized here. Input power is coupled to the device under test via a waveguide probe (waveguide to stripline transition) which extends into the WR-12 input waveguide. A stripline filter is integrated onto the waveguide probe to prevent power at harmonics above the fundamental from reaching the input waveguide. Near the device under test, a two-section quarter-wave impedance transformer is used to couple the reduced-height backshort waveguide to the WR-3 output waveguide. The transformer, spaced approximately a half wavelength from the plane of the device under test, acts as a reactive idler at the second harmonic frequency. The output waveguide is cut-off at both the fundamental and second harmonic frequencies. The block is equipped with three separate adjustable contacting short-circuit tuners (see Figures 7.10 and 7.11), a backshort tuner

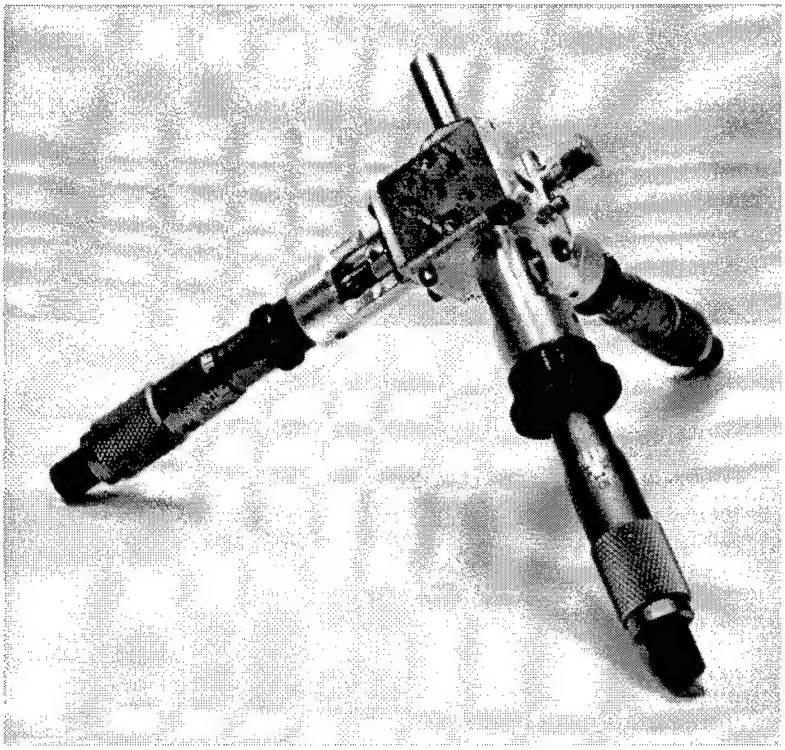
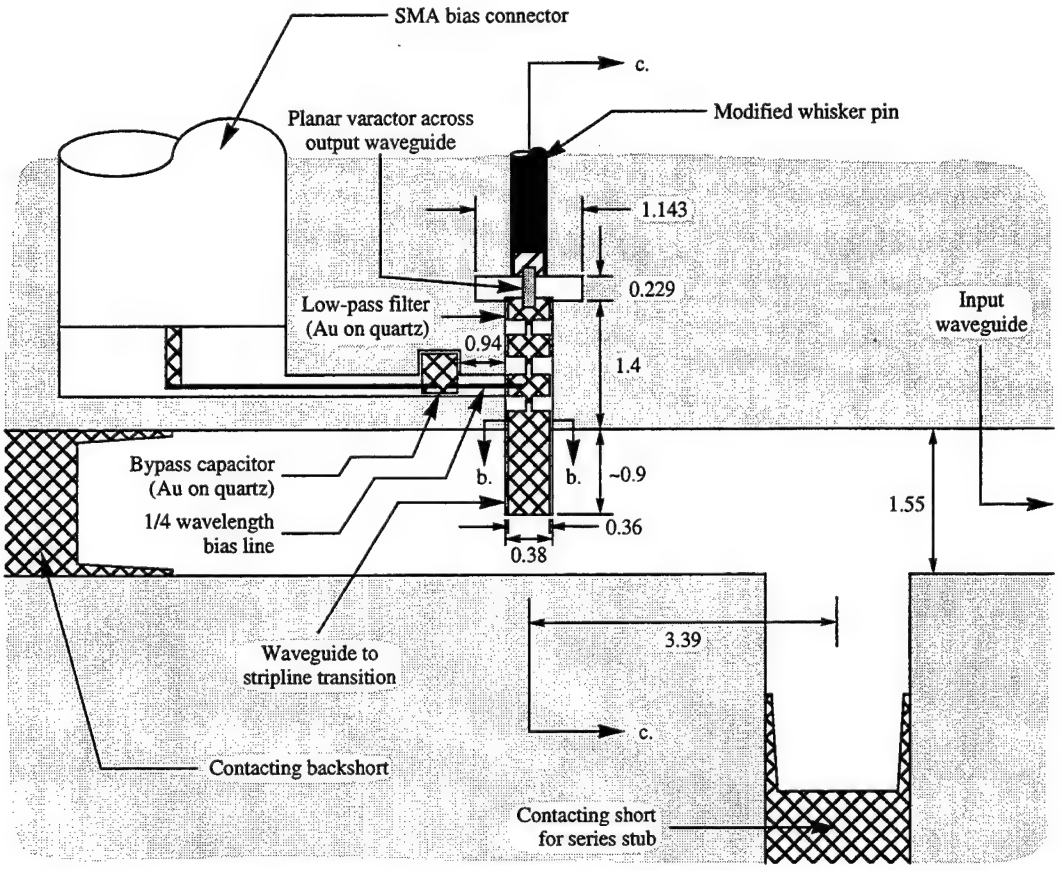
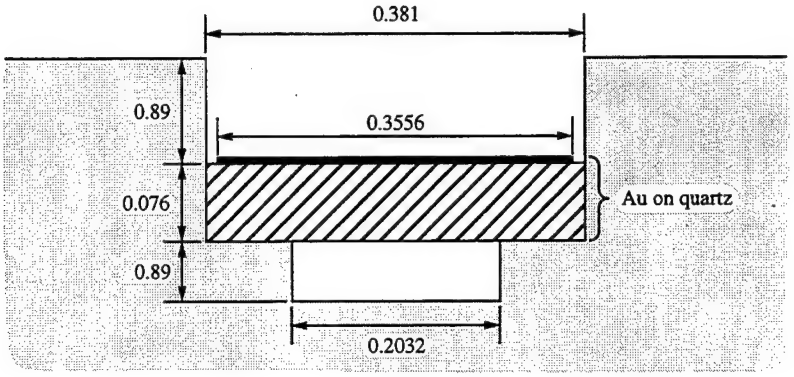


Figure 7.10 The NRAO A2621-TR2-T12 200-290 GHz tripler block fully assembled. The input waveguide can be seen on the front face of the block, while the output "horn" antenna can be seen at the top of the block. The output backshort micrometer can be seen in the foreground of the picture, while the input backshort micrometer can be seen in the background of the picture; the input E-plane micrometer is visible on the left-hand side of the picture.

and an E-plane tuner on the input waveguide as well as a backshort tuner on the output waveguide. It is important to note that the output waveguide backshort is utilized to tune both the output circuit at the third-harmonic frequency and the idler circuit at the second harmonic frequency. Finally, d.c. bias to the device under test is provided via a 140 Ω transmission line bias filter. The transmission line consists of a 1 mil diameter Au wire which is bonded between one of the low-impedance sections of the stripline filter and a 100 fF Au on quartz dielectric capacitor. The capacitor is enclosed in a rectangular shield machined into the block, and acts as an r.f. short-circuit which is transformed to an open-circuit at the stripline filter.

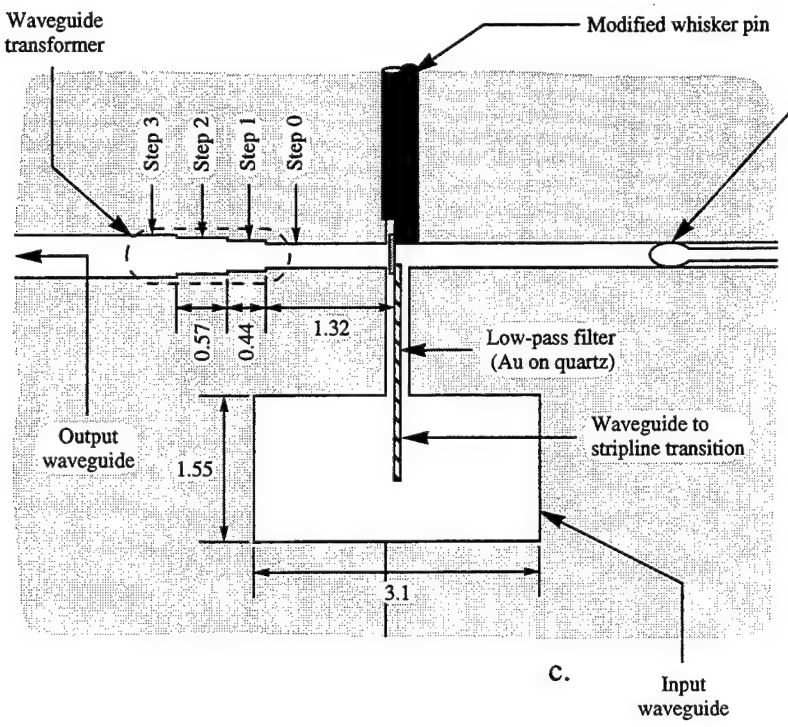


a.



b.

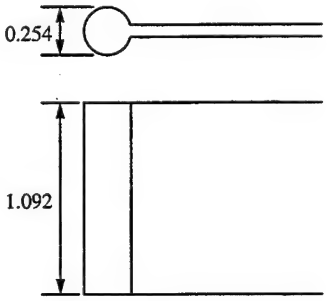
Figure 7.11 Schematic diagrams of the NRAO A2621-TR2-T12 200-290 GHz tripler block showing (a.) the block split along the partition between the block halves, (b.) a cross-section of the stripline filter channel, (c.) a cross-section through the block detailing the output waveguide transformer and device under test mounting configuration, and (d.) the configuration for the output backshort. Note that all dimensions are in millimeters.



c.

Waveguide Transformer Dimensions

Step	Width	Height
0	1.143	0.229
1	1.054	0.279
2	0.851	0.356
3	0.762	0.381



d.

Figure 7.11, continued.

An array of waveguide probe/stripline filter structures (ATR1) were fabricated for this work on 3 mil thick quartz using standard optical photolithography, metallization, and sputter etching procedures. First, a 50 Å/2000 Å Cr/Au "seed" layer was sputter deposited on the quartz substrate. After defining the array of stripline filter structures in photoresist, the Au filter structures were d.c. electroplated to a thickness of approximately 2.5 μm. After removing the photoresist, the exposed "seed" metallization was removed via an Ar sputter etch process. Finally, the substrate was diced to separate the individual circuits.

In order to support planar devices across the output waveguide (see Figure 7.11 (a.)), the whisker pin of the block was modified as outlined in reference [7.3]. This minor modification, which was performed by R. F. Bradley and N. Horner at NRAO, involved milling out a flat surface on the side of the whisker pin such that the milled out surface was in the plane of the top side of the stripline filter circuit. Ideally, the distance between the plane of this flat surface and the upper half of the block is approximately 3.5 mils (see Figure 7.11(b.)). As such, the planar HBVs of Chapter 6 were lapped to a thickness of about 2.25 mils to accommodate the combined heights of the epoxy used to secure the stripline circuit, the device, and the solder used to secure the device.

After wire bonding a long 1 mil Au wire to the last stripline filter circuit low impedance section (see Figure 7.11(a.)) and trimming the length of this Au wire to approximately 1.25 mm, the circuit was secured in the tripler block using a 90 minute curing epoxy. The free end of the Au wire was then wire bonded to the Au on quartz dielectric capacitor to complete the bias circuit. Finally, to accommodate device mounting, indium bumps were formed on the end of the stripline filter circuit and on the flat surface of the whisker pin using pure indium and SuperSafe Flux No. 3, and heating the block to approximately 160 °C until the indium melted. Planar HBVs were mounted across the output waveguide (Figure 7.11(a.) and (c.)) by pressing the devices into the indium bumps without heating the block. Since the planar HBVs were approximately 11.75 mils long and the stripline filter circuit extended into the output waveguide by about 2 mils (the whisker pin did not extend into the output waveguide), there was about 4.75 mils of overlap for mounting the devices. The author gratefully acknowledges the assistance of P. Koh in mounting the stripline filter circuit and planar HBVs in the tripler block.

7.3.2 Tripler Measurement Test Setup

The performance of planar HBV triplers was evaluated using three types of measurements: (1) output power versus frequency with 50 mW of input power, (2) output power versus input power at the frequency of highest tripling efficiency, and (3) input return loss versus frequency with 50 mW of input power. Except for output power versus input power measurements above 60 mW of input power, the test setup of Figure 7.12 was utilized for all measurements. Due to excessive losses in the circulator, waveguide switch,

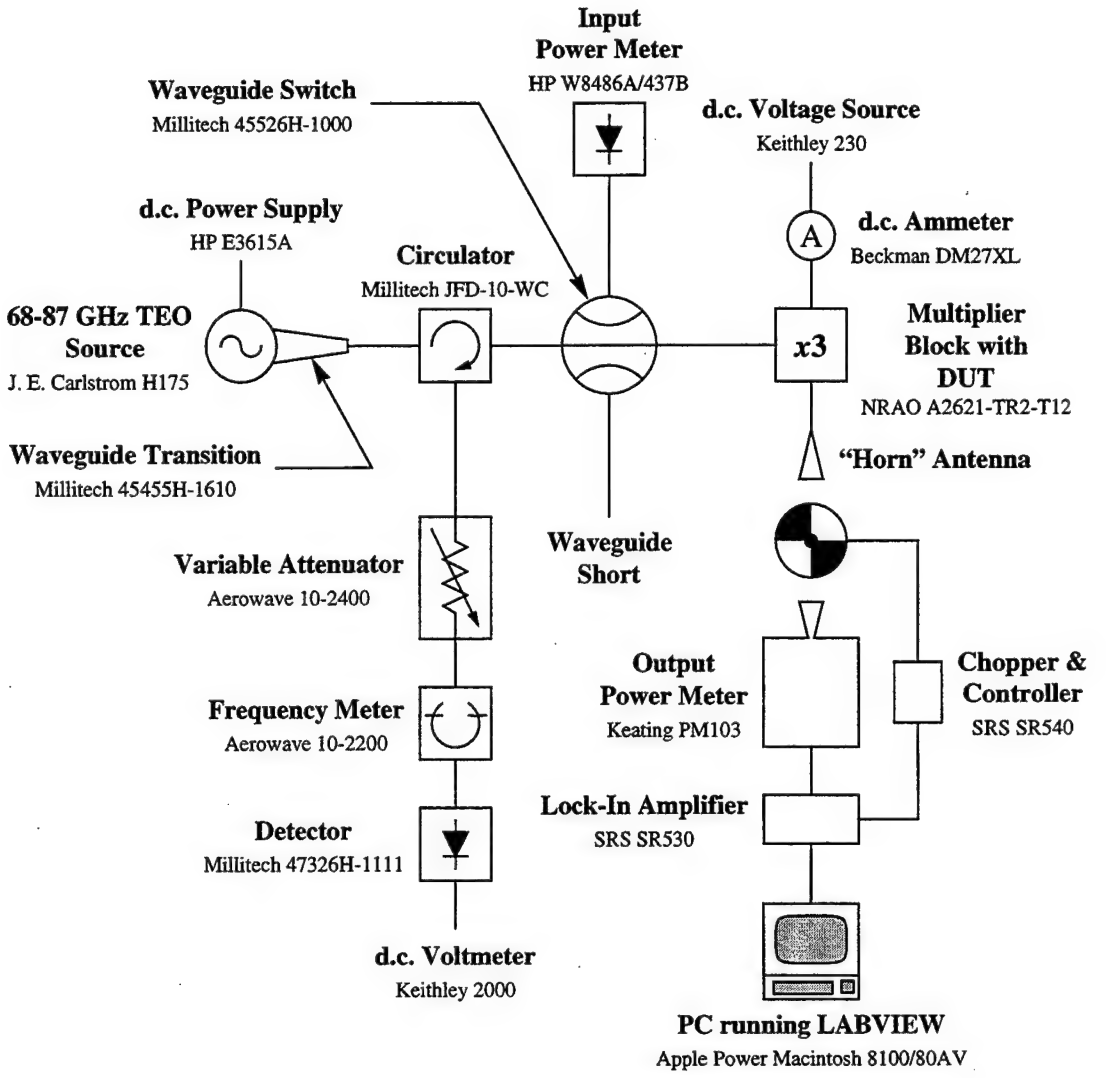


Figure 7.12 Test setup for measuring the performance of frequency multipliers.

and sections of waveguide between the input power source and the tripler block, the source was connected directly to the tripler block for output power versus input power measurements above 60 mW of input power.

The input power source for the measurement test setup of Figure 7.12 is a mechanically tuned, low noise Transferred Electron Oscillator (TEO) which produces up to 100 mW of power at frequencies from 68 GHz to 87 GHz. The amount of input power supplied to the multiplier block is controlled by an adjustable output waveguide backshort on the TEO cavity; the frequency of oscillation is controlled by an adjustable "top-hat" on

the cavity. The input power is measured using a Hewlett-Packard W8486A power sensor operating, from 75 GHz to 110 GHz, with a dynamic range of -30 dBm to 20 dBm. Finally, the output power from the tripler block is measured using a PM103 Terahertz Absolute Power Meter System manufactured by Thomas Keating, Ltd. The output power meter operates from 30 GHz to 3 THz, and employs a closed, air-filled cell detector to measure the power contained in incident free-space beams. The closed cell detector contains a metal film which absorbs a known fraction of the power incident on the cell. The incident beam is amplitude modulated by a chopper at a frequency of approximately 27 Hz such that the absorption of power in the metal film produces modulated variations in the temperature of the film. This, in turn, produces a modulation of the pressure in the cell which is detected by a pressure transducer. The output voltage from the pressure transducer is measured by a lock-in amplifier and represents the sensitivity of the power meter to the incident power. The meter is calibrated by generating a known amount of ohmic power in the metal film; the ohmic power is generated by passing a modulated current through the film at the same modulation frequency as that used to modulate the input beam. Manufacturer-supplied calibration factors account for loss in the meter's input "window" as a function of frequency, fractional film absorption, and fractional cell transmission. In order to eliminate reflections from the input "window", the meter is set so that the incident beam is oriented at the Brewster angle (55°) with the plane of polarization in the plane of incidence.

In order to accurately measure absolute power, it is important to ensure that all of the detected power comes from the incident beam. Since the Keating absolute power meter is very broadband, any modulated power from external thermal, optical, or acoustic sources will be detected. These "noise" sources were minimized by (1) minimizing the distances between the tripler output "horn" antenna, the chopper blade, and the detector, and (2) placing a sheet of absorptive material directly behind the chopper blade with only the tripler "horn" antenna passing through the sheet.

7.3.3 Tripler Measurement Procedure

An overview of the basic measurement procedure utilized in this work is given, in reference to Figure 7.12, below:

1. The TEO source, chopper, lock-in amplifier, input power meter, and output power meter are turned on and allowed to stabilize for 30 minutes.

2. The current-voltage (I-V) characteristic for the device under test is measured and recorded.

3. The input and output power meters are calibrated following standard operating procedures.

4. The TEO source is biased to -10.0 V.

5. The TEO source is tuned to the desired frequency by adjusting the length of the fundamental resonator on the cavity. The frequency is checked via the mechanical frequency meter with the waveguide switch set to the waveguide short-circuit. The variable attenuator is adjusted such that the detector diode is operating as a square-law detector.

6. The TEO source output power is set to the desired level via the adjustable output waveguide backshort and checked via the input power meter.

7. Steps 5 and 6 are repeated, as necessary.

8. The waveguide switch is set to the waveguide short, the variable attenuator is adjusted such that the detector diode is operating as a square-law detector, and the detected voltage and attenuation factor are recorded.

8. The HBV under test is biased to 0.0 V and the waveguide switch is set to the tripler block.

9. The tripler block input tuners are adjusted for maximum output power from the block.

10. The tripler block output tuners are adjusted for maximum output power from the block.

11. Steps 9 and 10 are repeated, as necessary.

12. Once the maximum output power from the tripler block is achieved for a given frequency and input power level, the output power, input/output tuner positions, and d.c. rectified current are recorded. In addition, the variable attenuator is adjusted such that the detector diode is operating as a square law detector, and the detected voltage and attenuation factor are recorded. The input return loss of the tripler block, defined as

$$RL_{input} = 10\log\left(\frac{\text{Reflected power from tuned tripler}}{\text{Reflected power from waveguide short}}\right), \qquad (7.1)$$

can be determined from the detected voltages and attenuation factors of the present step and step 8.

13. The input power level or frequency is adjusted (see steps 5-7) and steps 8-12 are repeated until a range of input power levels or frequencies has been covered.

7.3.4 Tripler Results for the UVA-NRL-1174 Planar HBV

The performance of the prototype planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV triplers of Chapter 6 was evaluated near the 80/240 GHz center frequency of the NRAO tripler block described in *Section 7.3.1*. Devices with nominal anode diameters of 10 μm (approximately 8.75 μm after wet etching) were tested. For an input (available) power of 50 mW, the output power versus fundamental frequency for frequencies between 76 GHz and 85.5 GHz is shown in Figure 7.13. More than 1 mW of power was generated at fundamental frequencies between approximately 81.5 GHz and 85.25 GHz. As shown in Figure 7.14, the input return loss for these measurements was better than -10 dB for fundamental frequencies between about 71.5 GHz and 85 GHz. At a fundamental frequency of 84 GHz, the output power versus available power is shown in Figure 7.15. A maximum output power of greater than 2 mW was generated at 252 GHz with an available power of 80 mW, yielding a peak flange-to-flange tripling efficiency of greater than 2.5 %. The device d.c. rectified current versus available power is shown in Figure 7.16; this data corresponds to the measurements of Figure 7.15. From this figure, it is clear that the symmetry in the UVA-NRL-1174 material and device structures is quite good since the device d.c. rectified current is fairly low. For historical comparison purposes, the initial whisker-contacted single barrier HBVs of reference [7.4] had a maximum output power (tripling efficiency) of approximately 1.25 mW (5 %) at an output frequency of 228 GHz (225 GHz). At an output frequency of 252 GHz, the maximum output power was only 1 mW with a tripling efficiency of only 3 %. Subsequent tests using these same whisker-contacted single barrier HBVs in a second tripler block yielded a maximum output power (tripling efficiency) of only about 0.8 mW (2 %) at an output frequency of 192 GHz[7.5].

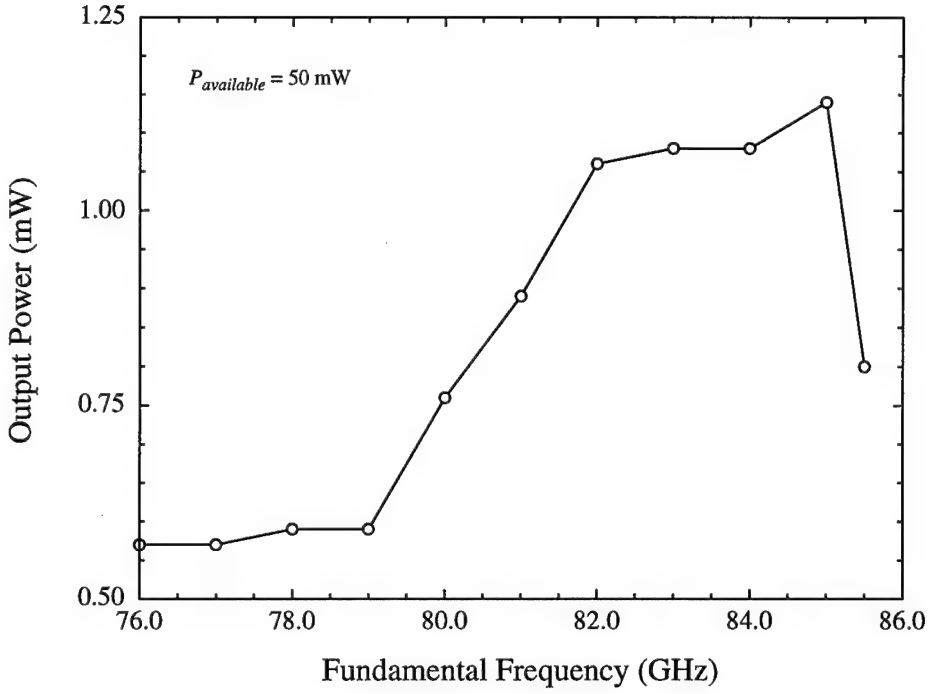


Figure 7.13 Output power versus fundamental frequency for the prototype planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV triplers (UVA-NRL-1174-K) of Chapter 6 at an available power of 50 mW.

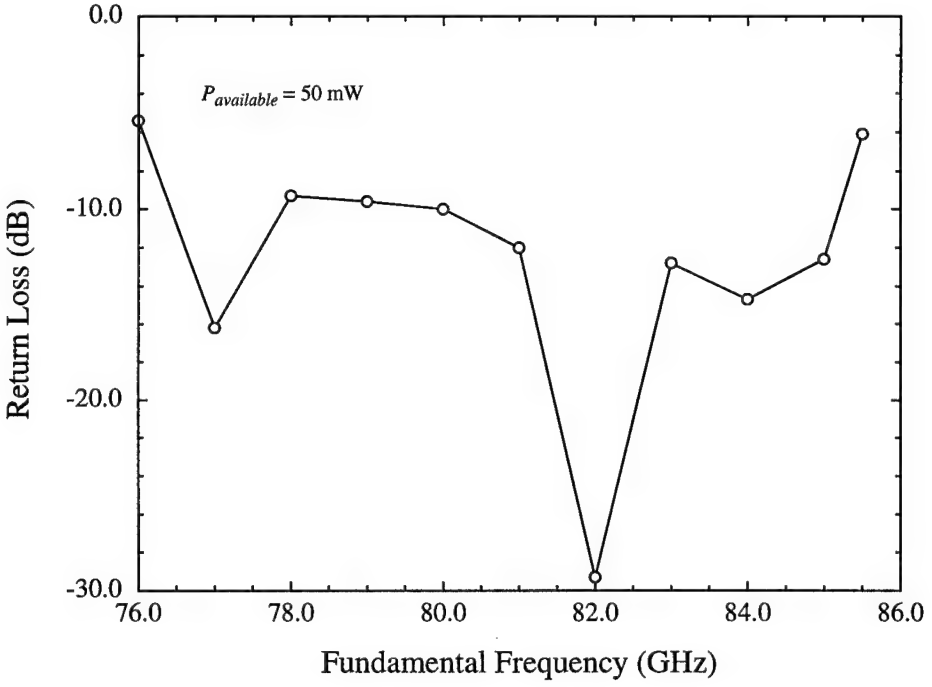


Figure 7.14 Input return loss versus fundamental frequency for the prototype planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV triplers (UVA-NRL-1174-K) of Chapter 6 at an available power of 50 mW.

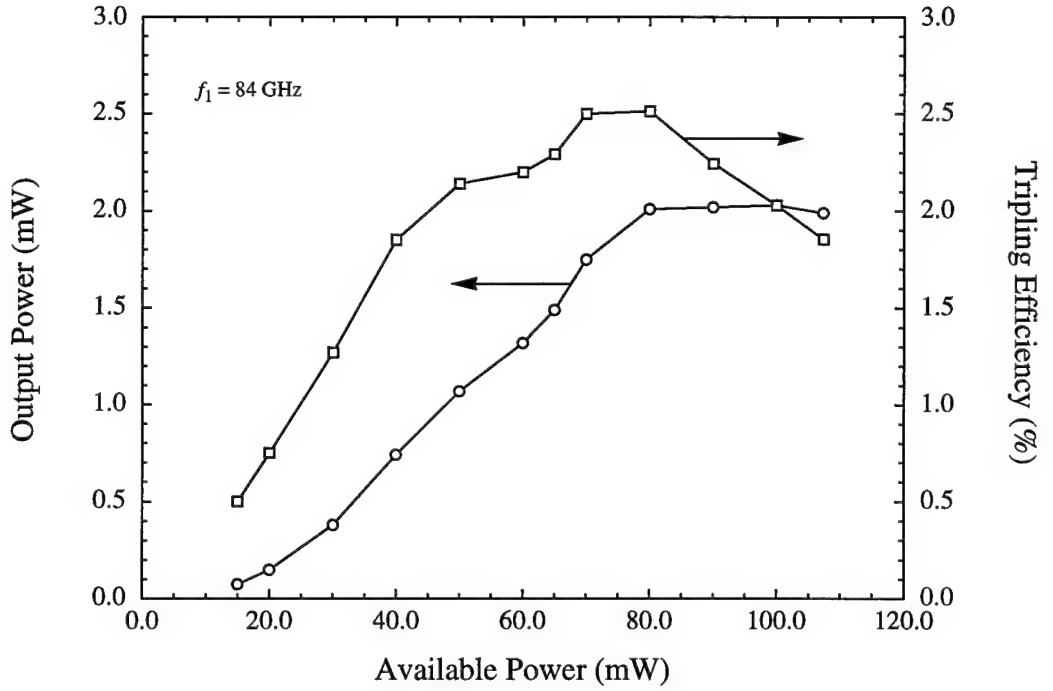


Figure 7.15 Output power versus available power for the prototype planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV triplers (UVA-NRL-1174-K) of Chapter 6 at a fundamental (output) frequency of 84 GHz (252 GHz).

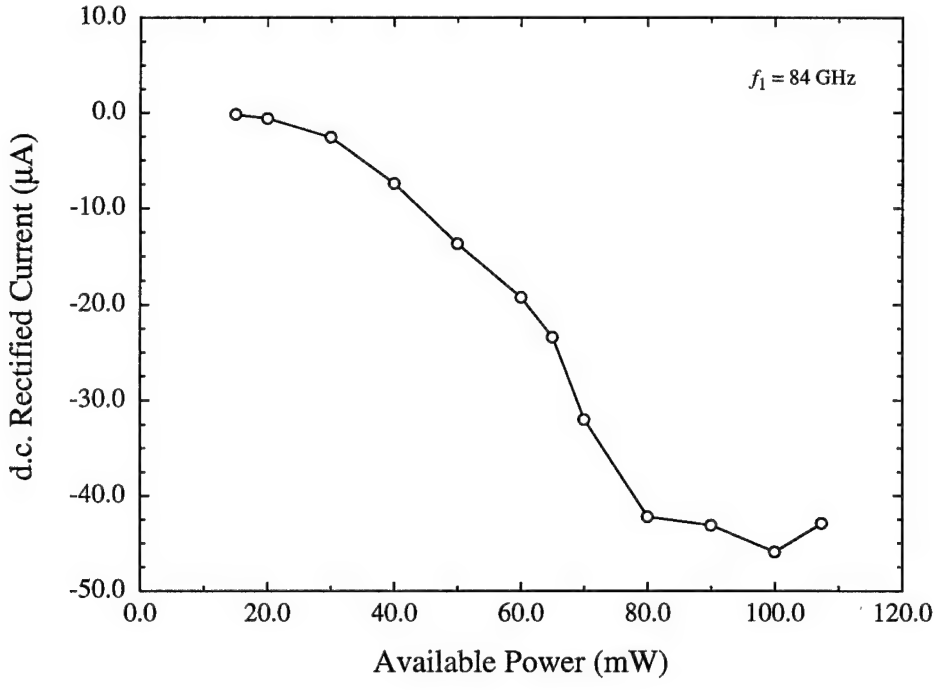


Figure 7.16 Device d.c. rectified current versus available power for the prototype planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBV triplers (UVA-NRL-1174-K) of Chapter 6 at a fundamental (output) frequency of 84 GHz (252 GHz).

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Chapter 8

Summary, Conclusions, and Future Work

8.1 Research Summary and Conclusions

The major goals of this research were (1) the development of accurate and fully self-consistent computer-aided analysis and design techniques for millimeter wave frequency multiplier devices and circuits, and (2) the design, fabrication, and testing of state-of-the-art planar Heterostructure Barrier Varactor (HBV) frequency triplers operating near 200 GHz that are suitable for use in quasi-optical HBV frequency tripler arrays.

In order to effectively design millimeter and submillimeter wave frequency multipliers, techniques were developed to analyze both the electrical and thermal properties of the device and circuit in a fully self-consistent manner. In particular, large-signal time- and temperature-dependent numerical device simulators were developed for generic heteroepitaxial InGaAs/InAlAs on InP, InGaAs/InP on InP, and GaAs/InGaAs/AlGaAs on GaAs HBV structures. Although the present focus was on HBVs and SBVs, the general transport formulation/numerical solution technique presented in this dissertation is applicable to all unipolar devices having ohmic and/or Schottky contacts, and which contain regions of smoothly varying alloy composition interrupted by a finite number of abrupt material discontinuities. The numerical device simulators are based on the drift-diffusion equations, and self-consistently combine current transport through the device bulk with current across the abrupt heterointerfaces or metal-semiconductor interface. Given the importance of both the nonlinear device and its embedding circuit, the device simulators were combined with a novel and efficient harmonic-balance circuit analysis technique. In conjunction with the combined numerical device/harmonic-balance circuit analysis, the steady-state thermal properties of whisker-contacted and planar geometry frequency multiplier circuits were analyzed based on the amount of power dissipated in the active region of the device and the thermal resistance to heat flow presented by the various elements that make up the circuit. From these quantities the average temperature across the active region of the varactor can be estimated for use in the appropriate device simulator.

Excellent correlation has been obtained between the HBV device simulator and experimental d.c. I-V and static C-V characteristics for several GaAs/AlGaAs and GaAs/InGaAs/AlGaAs HBVs. The combined numerical device/harmonic-balance circuit simulators for both HBVs and SBVs have been compared to published experimental r.f. results, as well as to harmonic-balance results utilizing quasi-static equivalent circuit device models. These comparisons accentuate the importance of using a numerical device model in place of the standard quasi-static equivalent circuit device model for the design and analysis of frequency multipliers, particularly at millimeter and submillimeter wavelengths where the large-signal nonstationary high frequency dynamics of carrier transport begin to dominate device operation. Only the general approach presented in this dissertation allows for the accurate and self-consistent modeling of such large-signal dynamic effects as current saturation, the bias-dependent parasitic impedance and shunting capacitance of device undepleted regions, electron velocity saturation, and electron mass-inertial effects[8.1 - 8.10]. Again, it is the belief of the author that analysis and design approaches as advocated in this work are essential to the development of efficient and reliable circuits operating into the terahertz frequency range.

Based on extensive d.c. and large-signal HBV simulations, planar four barrier GaAs/$Al_{0.7}Ga_{0.3}As$ HBVs were designed for tripling from 80 GHz to 240 GHz. Prototype devices were fabricated using a process in which the device "surface channel" is etched prior to the formation of the contact pad-to-anode "finger". Formation of the device "finger" after etching the "surface channel" is facilitated by a trench planarization technique, and yields a device with minimal parasitic capacitances. This process is directly applicable to the fabrication of quasi-optical HBV frequency tripler arrays. Planar four barrier HBV triplers with nominal 10 μm diameter anodes were tested in a crossed-waveguide tripler block; as much as 2 mW of power was generated at 252 GHz with a flange-to-flange tripling efficiency of 2.5 %. These devices are the first planar or multi-barrier HBVs reported, and their tripling performance exceeds that of previous whisker-contacted single barrier HBVs[8.11, 8.12].

In summary, the following items highlight the important research accomplishments presented in this dissertation:

1. Development of the first integrated drift-diffusion device/harmonic-balance circuit simulator for the large-signal nonlinear analysis HBV and SBV frequency multiplier circuits.

2. Development of a detailed steady-state thermal model for the analysis of frequency multiplier thermal properties, and inclusion of thermal effects in the integrated device/circuit simulator via temperature-dependent device material parameters.

3. Development of a low-parasitic planar device fabrication process that is suitable for use with existing planar Schottky diode fabrication processes, and is directly applicable to the fabrication of quasi-optical HBV frequency tripler arrays.

4. Fabrication of the first planar multi-barrier HBVs for frequency tripling from 80 GHz to 240 GHz, and demonstration of state-of-the-art planar HBV frequency tripler performance that exceeds the performance of previous whisker-contacted HBV triplers (greater than 2 mW of output power at 252 GHz with a flange-to-flange peak tripling efficiency of 2.5 %).

8.2 Suggestions for Future Research

8.2.1 Large-Signal Numerical Device/Harmonic-Balance Circuit Analysis

Although the present research has significantly advanced the state-of-the-art in large-signal nonlinear analysis of frequency multipliers, several recommendations can be made to improve on this work. As noted in Chapter 5, the use of a field-dependent electron mobility in the SBV numerical device/harmonic-balance circuit simulator had a dramatic effect on SBV simulation results. These results suggest that the electron mobility is drive and frequency dependent, and should be determined from large-signal sinusoidal Monte Carlo simulations rather than the usual static Monte Carlo simulations[8.7]. The determination of large-signal, high frequency transport parameters for varactor devices from large-signal sinusoidal Monte-Carlo simulations, and evaluation of how these parameters affect the numerical device/harmonic-balance circuit simulations would be quite useful. For short devices or for simulations at frequencies above about 300 GHz, the use of an alternate carrier transport formulation (full momentum/energy balance or Monte Carlo) in conjunction with the harmonic-balance circuit analysis would be required to accurately account for hot electron effects. For varactor simulations at high input power

levels, the inclusion of avalanche breakdown phenomena in the numerical device simulator is imperative. Despite the fact that the inclusion of such phenomena would require the simulation of both electron and hole transport, it is thought that the resulting simulator would have better convergence properties than the current simulators due to the presence of additional diagonal terms in the Jacobian matrix used to solve the transport equations.

Despite the fact that the majority of the numerical device/harmonic-balance circuit simulations presented in this dissertation utilized the Accelerated Fixed-Point (AFP) harmonic-balance algorithm, there were instances where this algorithm failed and the basic unaccelerated harmonic-balance algorithm (equation (3.1)) was required. Further development of the AFP method is clearly necessary to expand its usefulness. In particular, a full evaluation of the convergence properties of the method would be useful; such an evaluation should include investigating the appropriate number of harmonics to include in the analysis, determining the best convergence criteria in terms of simulation accuracy and speed, and investigating the use of variable transmission line impedances at the different harmonics. Improvements in the acceleration algorithm may also be possible by utilizing a multi-dimensional scheme in which a specific harmonic voltage update is based on a sequence of voltage iterates from multiple harmonics.

Automation of the numerical device/harmonic-balance circuit optimization process would be extremely useful. At present, design optimization is done manually by running, on a group of computer workstations, a set of simulations with different device embedding impedances and/or device physical parameters with all simulations starting from the same equilibrium condition. The use of a sophisticated numerical optimization scheme would certainly improve the speed of such optimizations, and the use of a parallel process computation environment such as the University of Virginia MENTAT environment[8.13, 8.14] would simplify these optimizations by automating the multi-workstation simulation process.

As noted in Chapter 5, the discrepancies between frequency multiplier experimental results and the results obtained from numerical device/harmonic-balance multiplier circuit simulations are attributed mainly to a lack of knowledge about the actual impedances presented to an active device by the multiplier circuit in which it is embedded.

The accurate determination of active device embedding impedances (for example, the impedances of waveguide mounting structures such as the one described in Chapter 7) would greatly improve the analysis and design of frequency multiplier circuits. Recent work to determine the embedding impedances of SBV doubler blocks[8.15, 8.16] and Transferred Electron Oscillator (TEO) waveguide cavities[8.17] using a three-dimensional finite-element electromagnetic simulator[8.18] suggests that it is now feasible to determine these impedances for a wide range of waveguide mounting structures. Overall, the use of a numerical device/harmonic-balance circuit simulation technique in conjunction with an electromagnetic simulation scheme would facilitate the complete development of high efficiency frequency multiplier circuits based on the co-design of both the active device and its embedding circuitry, be it a waveguide multiplier block or a quasi-optical multiplier array.

Finally, the large-signal numerical device/harmonic-balance circuit analysis techniques developed for the present research could be applied to the analysis of mixers by developing a small-signal mixer model. Such a model would be quite easy to develop as it would be based on the large-signal mixer conductance and capacitance waveforms obtained from the large-signal numerical device/harmonic-balance circuit simulators.

8.2.2 Design and Fabrication of Heterostructure Barrier Devices

In the area of design and fabrication, several things can be done to improve upon the HBV tripler results presented in Chapter 7. First, a more aggressive device design that accounts for electron velocity saturation can be used to lower the parasitic impedance of the device active region. Second, a material structure with a larger barrier height (larger modulation region/barrier region conduction-band differential) can be used to reduce the parasitic conduction current through the device active region. Lastly, a tripler block optimized for the HBV, that is one without a second harmonic idler termination, can be used. In addition to frequency triplers, the development of relatively efficient higher order, odd harmonic frequency multipliers should be possible due to need for only odd harmonic idler terminations. Finally, the development of high power quasi-optical HBV tripler arrays is a natural extension of the present research. The planar device fabrication process utilized here is directly applicable to the fabrication of small quasi-optical tripler arrays. More

importantly, the design of such tripler arrays would be greatly simplified by the fact that neither idler circuits nor d.c. bias for the individual devices (array elements) would be required.

Chapter 8 References

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Appendix A

Heterostructure Barrier and Schottky Barrier Varactor Device Simulation Via the Newton-Raphson Method

This appendix catalogs the normalized and discretized versions of the time-dependent state equations, interface constraints, and boundary constraints, for both Heterostructure Barrier Varactors (HBVs) and Schottky Barrier Varactors (SBVs), that were presented in Chapter 2. A detailed description of the Newton-Raphson numerical technique utilized to solve the resulting two-point boundary value problem is also given in this appendix.

A.1 Normalized and Temporally Discretized State Equations, Interface Constraints, and Boundary Constraints

Following the discussion in *Section 2.2*, the time-dependent state equations, interface constraints, and boundary constraints, presented in *Sections 2.1.1-2.1.4* for both single barrier HBVs and SBVs, are given below in their normalized and temporally discretized form following reference [A.1].

A.1.1 Heterostructure Barrier Varactor

For a single barrier HBV, the normalized and temporally discretized state equations are

$$F_1^k = \frac{d\psi_1^k}{dx} + \frac{D_1^k(x)}{\varepsilon_1(x)} = 0, \tag{A.1}$$

$$F_2^k = \frac{dD_1^k}{dx} + n_{i,ref} \exp\left[\psi_1^k(x) + V_{n,1}(x) - \phi_{n,1}^k(x)\right] - N_{D,1}(x) = 0, \tag{A.2}$$

$$F_3^k = \frac{d\phi_{n,1}^k}{dx} + \frac{J_{n,1}^k(x)}{\mu_{n,1}^k(x)\, n_{i,ref} \exp\left[\psi_1^k(x) + V_{n,1}(x) - \phi_{n,1}^k(x)\right]} = 0, \tag{A.3}$$

$$F_4^k = \frac{dJ_{n,1}^k}{dx} - \frac{n_{i,ref}\exp\left[\psi_1^k(x) + V_{n,1}(x) - \phi_{n,1}^k(x)\right] - n_1^{k-1}}{\Delta t} = 0, \tag{A.4}$$

$$F_5^k = \frac{d\psi_2^k}{dx} + \left\{\frac{D_2^k(x)}{\varepsilon_2(x)}\right\} S_1 = 0, \tag{A.5}$$

$$F_6^k = \frac{dD_2^k}{dx} + \left\{n_{i,ref}\exp\left[\psi_2^k(x) + V_{n,2}(x) - \phi_{n,2}^k(x)\right] - N_{D,2}(x)\right\} S_1 = 0, \tag{A.6}$$

$$F_7^k = \frac{d\phi_{n,2}^k}{dx} + \left\{\frac{J_{n,2}^k(x)}{\mu_{n,2}^k(x)\, n_{i,ref}\exp\left[\psi_2^k(x) + V_{n,2}(x) - \phi_{n,2}^k(x)\right]}\right\} S_1 = 0, \tag{A.7}$$

$$F_8^k = \frac{dJ_{n,2}^k}{dx} - \left\{\frac{n_{i,ref}\exp\left[\psi_2^k(x) + V_{n,2}(x) - \phi_{n,2}^k(x)\right] - n_2^{k-1}}{\Delta t}\right\} S_1 = 0, \tag{A.8}$$

$$F_9^k = \frac{d\psi_3^k}{dx} + \left\{\frac{D_3^k(x)}{\varepsilon_3(x)}\right\} S_2 = 0, \tag{A.9}$$

$$F_{10}^k = \frac{dD_3^k}{dx} + \left\{n_{i,ref}\exp\left[\psi_3^k(x) + V_{n,3}(x) - \phi_{n,3}^k(x)\right] - N_{D,3}(x)\right\} S_2 = 0, \tag{A.10}$$

$$F_{11}^k = \frac{d\phi_{n,3}^k}{dx} + \left\{\frac{J_{n,3}^k(x)}{\mu_{n,3}^k(x)\, n_{i,ref}\exp\left[\psi_3^k(x) + V_{n,3}(x) - \phi_{n,3}^k(x)\right]}\right\} S_2 = 0, \tag{A.11}$$

and

$$F_{12}^k = \frac{dJ_{n,3}^k}{dx} - \left\{\frac{n_{i,ref}\exp\left[\psi_3^k(x) + V_{n,3}(x) - \phi_{n,3}^k(x)\right] - n_3^{k-1}}{\Delta t}\right\} S_2 = 0 \tag{A.12}$$

where k signifies the present time step. The state variables in these equations are numbered relative to the three regions shown in Figure A.1, while the domain of the equations is $x_{B1} \le x \le x_{B2}$ as shown in this figure. This device domain mapping yields the state equation scaling factors

$$S_1 = \frac{(x_{h1} + 1) - (x_{h2} - 1)}{x_{h1} - x_{cathode}} \tag{A.13}$$

and

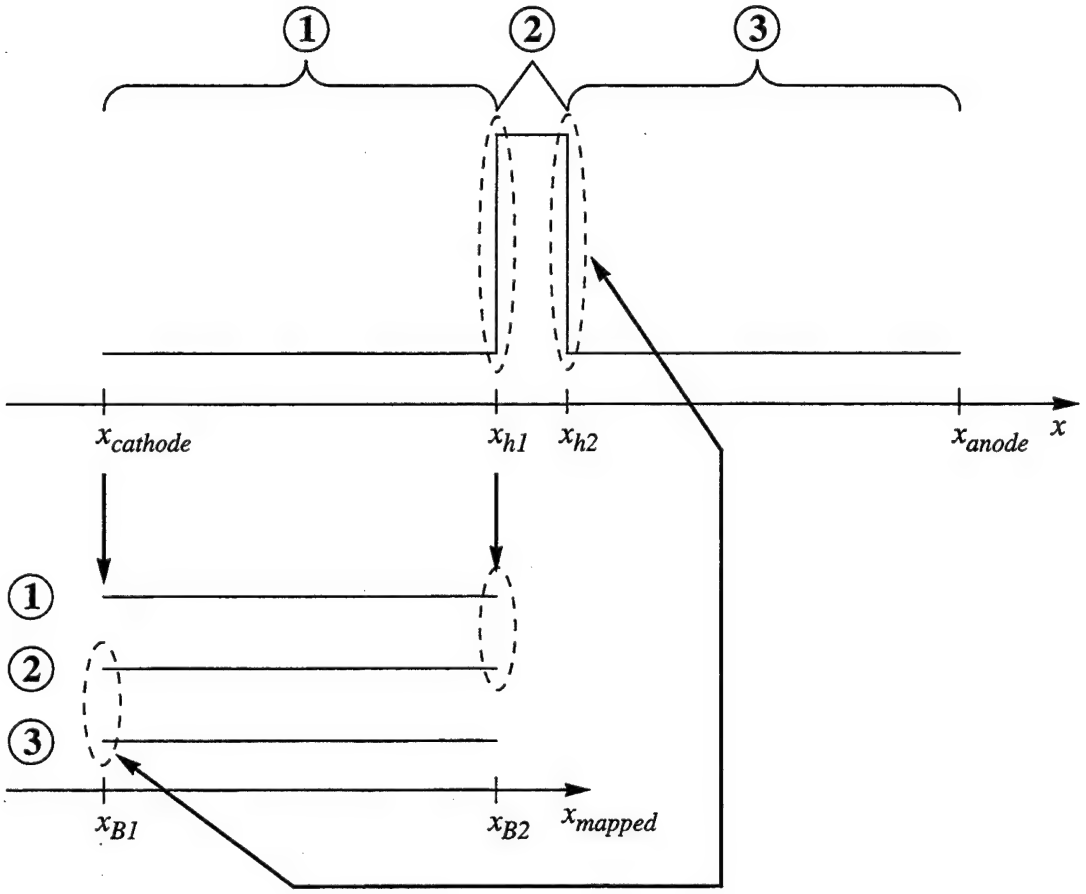

Figure A.1 Schematic representation of the HBV device domain mapping procedure required for the utilization of existing numerical codes which solve two-point boundary value problems.

$$S_2 = \frac{x_{anode} - x_{h2}}{x_{h1} - x_{cathode}}. \tag{A.14}$$

Furthermore, the material parameters in the three regions of the device, designated by the generic parameters ζ_1, ζ_2, and ζ_3, are mapped as follows

$$\zeta_1(x_{mapped}) = \zeta(x) \tag{A.15}$$

$$\zeta_2(x_{mapped}) = \zeta(S_1(x - x_{cathode}) + x_{h2} - 1) \tag{A.16}$$

$$\zeta_3(x_{mapped}) = \zeta(S_2(x - x_{cathode}) + x_{h2}) \tag{A.17}$$

where $x_{B1} \le x_{mapped} \le x_{B2}$ and $x_{cathode} \le x \le x_{h1}$ such that these two ranges are equivalent. It is important to note that the left heterointerface is chosen to lie midway between the x_{h1} and $x_{h1} + 1$ grid points. Likewise, the right heterointerface is chosen to lie midway between the $x_{h2} - 1$ and x_{h2} grid points.

As a consequence of device domain mapping, the heterointerface constraints for a single barrier HBV are transformed into boundary constraints. The resulting constraints at the $x_{B1} = x_{cathode}$ boundary are

$$G_1^k = \psi_1^k(x_{B1}) - V_{applied}^k + V_{n,1}(x_{B1}) - \ln\left[\frac{N_{D,1}(x_{B1})}{n_{i,ref}}\right] = 0, \tag{A.18}$$

$$G_2^k = \phi_{n,1}^k(x_{B1}) - V_{applied}^k = 0, \tag{A.19}$$

$$G_3^k = \psi_2^k(x_{B1}) - \psi_3^k(x_{B1}) = 0, \tag{A.20}$$

$$G_4^k = D_2^k(x_{B1}) - D_3^k(x_{B1}) = 0, \tag{A.21}$$

$$G_5^k = J_{n,2}^k(x_{B1}) - J_{n,3}^k(x_{B1}) = 0, \tag{A.22}$$

and

$$G_6^k = \begin{cases} J_{n,2}^k(x_{B1}) - \upsilon_{th1}\{\exp([\phi_{n,2}^k(x_{B1}) - \phi_{n,3}^k(x_{B1})] - 1)\} \\ \qquad \times n_{i,ref} \exp[\psi_2^k(x_{B1}) + V_{n,2}(x_{B1}) - \phi_{n,2}^k(x_{B1})] = 0, & V_{applied}^k \ge 0 \\ \exp[\phi_{n,2}^k(x_{B1}) - \phi_{n,3}^k(x_{B1})] - \exp\left[-\left(\frac{\upsilon_{d,1}^k}{c_{BC}}\right)^2\right] \\ \qquad + \left(\frac{2\sqrt{\pi}\upsilon_{d,1}^k}{c_{BC}}\right)\left(1 - \mathrm{erf}\left[\frac{\upsilon_{d,1}^k}{c_{BC}}\right]\right) = 0, & V_{applied}^k \le 0 \end{cases} \tag{A.23}$$

while the constraints at the $x_{B2} = x_{h1}$ boundary are

$$G_7^k = \psi_3^k(x_{B2}) + V_{n,3}(x_{B2}) - \ln\left[\frac{N_{D,3}(x_{B2})}{n_{i,ref}}\right] = 0, \tag{A.24}$$

$$G_8^k = \phi_{n,3}^k(x_{B2}) = 0, \tag{A.25}$$

$$G_9^k = \psi_1^k(x_{B2}) - \psi_2^k(x_{B2}) = 0, \tag{A.26}$$

$$G_{10}^k = D_1^k(x_{B2}) - D_2^k(x_{B2}) = 0, \tag{A.27}$$

$$G_{11}^k = J_{n,1}^k(x_{B2}) - J_{n,2}^k(x_{B2}) = 0, \tag{A.28}$$

and

$$G_{12}^k = \begin{cases} \exp\left[\phi_{n,2}^k(x_{B2}) - \phi_{n,1}^k(x_{B2})\right] - \exp\left[-\left(\dfrac{\upsilon_{d,2}^k}{c_{BC}}\right)^2\right] \\ \qquad + \left(\dfrac{2\sqrt{\pi}\upsilon_{d,2}^k}{c_{BC}}\right)\left(1 - \operatorname{erf}\left[\dfrac{\upsilon_{d,2}^k}{c_{BC}}\right]\right) = 0, \qquad V_{applied}^k \geq 0 \\ J_{n,2}^k(x_2) - \upsilon_{th2}\left\{\exp\left(\left[\phi_{n,2}^k(x_{B2}) - \phi_{n,1}^k(x_{B2})\right] - 1\right)\right\} \\ \qquad \times n_{i,ref} \exp\left[\psi_2^k(x_{B2}) + V_{n,2}(x_{B2}) - \phi_{n,2}^k(x_{B2})\right] = 0, \qquad V_{applied}^k \leq 0 \end{cases} \tag{A.29}$$

where

$$\upsilon_{th1} = \frac{L_D}{D_0}\frac{A^* T^2}{qN_c(x_{B1})}, \tag{A.30}$$

$$\upsilon_{th2} = \frac{L_D}{D_0}\frac{A^* T^2}{qN_c(x_{B2})}, \tag{A.31}$$

$$\upsilon_{d,1}^k = \frac{-J_{n,2}^k(x_{B1})}{n_{i,ref} \exp\left[\psi_2^k(x_{B1}) + V_{n,2}(x_{B1}) - \phi_{n,2}^k(x_{B1})\right]}, \tag{A.32}$$

$$\upsilon_{d,2}^k = \frac{J_{n,2}^k(x_{B2})}{n_{i,ref} \exp\left[\psi_2^k(x_{B2}) + V_{n,2}(x_{B2}) - \phi_{n,2}^k(x_{B2})\right]}, \tag{A.33}$$

and

$$c_{BC} = \frac{L_D}{D_0}\sqrt{\frac{2kT}{m_{D\text{-}M}^*}}. \tag{A.34}$$

A.1.2 Schottky Barrier Varactor

For a SBV, the normalized and temporally discretized state equations are

$$F_1^k = \frac{d\psi^k}{dx} + \frac{D^k(x)}{\varepsilon(x)} = 0 \tag{A.35}$$

$$F_2^k = \frac{dD^k}{dx} + n_{i,\,ref} \exp\left[\psi^k(x) + V_n(x) - \phi_n^k(x)\right] - N_D(x) = 0 \tag{A.36}$$

$$F_3^k = \frac{d\phi_n^k(x)}{dx} + \frac{J_n^k(x)}{\mu_n^k(x)\, n_{i,\,ref} \exp\left[\psi^k(x) + V_n(x) - \phi_n^k(x)\right]} = 0 \tag{A.37}$$

$$F_4^k = \frac{dJ_n^k}{dx} - \frac{n_{i,\,ref} \exp\left[\psi^k(x) + V_n(x) - \phi_n^k(x)\right] - n^{k-1}}{\Delta t} = 0 \tag{A.38}$$

where, again, k signifies the present time step. The boundary constraints at the metal-semiconductor interface (x_{B1}) are

$$G_1^k = \psi^k(x_{B1}) - \frac{\chi_{ref} - \Phi_{mwf}}{q} - \ln\left[\frac{N_{C,\,ref}}{n_{i,\,ref}}\right] - \frac{1}{V_{th}}\sqrt{\frac{q\left|D^k(x_{B1})\right|}{4\pi\varepsilon^2(x_{B1})}} = 0 \tag{A.39}$$

and

$$G_2^k = J_n^k(x_{B1}) - \upsilon_{rn}^k \left\{ n_{i,\,ref} \exp\left(\left[\psi^k(x_{B1}) + V_n(x_{B1}) - \phi_n^k(x_{B1})\right] - n_0 \right) \right\} = 0 \tag{A.40}$$

where

$$\upsilon_{rn}^k = \upsilon_d^k + \frac{c_{BC}}{\sqrt{\pi}} \left(\frac{\exp\left[-\left(\frac{\upsilon_d^k}{c_{BC}} \right)^2 \right]}{1 + \operatorname{erf}\left[\frac{\upsilon_d^k}{c_{BC}} \right]} \right), \tag{A.41}$$

$$\upsilon_d^k = \frac{-J_n^k(x_{B1})}{n_{i,\,ref} \exp\left[\psi^k(x_{B1}) + V_n(x_{B1}) - \phi_n^k(x_{B1})\right]}, \tag{A.42}$$

and

$$c_{BC} = \frac{L_D}{D_0}\sqrt{\frac{2kT}{m^*}}; \tag{A.43}$$

the boundary constraints at the ohmic contact (x_{B2}) are

$$G_3^k = \psi^k(x_{B2}) - V_{applied}^k + V_n(x_{B2}) - \ln\left[\frac{N_D(x_{B2})}{n_{i,ref}}\right] = 0 \tag{A.44}$$

and

$$G_4^k = \phi_n^k(x_{B2}) - V_{applied}^k = 0. \tag{A.45}$$

A.2 Finite-Difference Spatial Discretization Scheme

The finite-difference spatial discretization scheme utilized for the normalized time-dependent state equations is a second-order accurate trapezoidal-rule approximation over a nonuniform mesh having N+1 grid points. As a result, the temporally discretized state equations of *Section A.1*, which are of the form

$$F_i^k(x, y^k(x)) = \frac{dy_i^k}{dx} - f_i^k(x, y^k(x)) = 0, \tag{A.46}$$

take on the temporally and spatially discretized form

$$F_{i,j}^k = y_{i,j+1}^k - y_{i,j}^k - \frac{h_j}{2}[f_i^k(x_j, y_j^k) + f_i^k(x_{j+1}, y_{j+1}^k)] = 0 \tag{A.47}$$

where $j = 1, 2, 3, \ldots, N$, $i = 1, 2, 3, \ldots, m$ ($m = 12$ for HBVs and $m = 4$ for SBVs), and $y^k = (y_1^k, y_2^k, y_3^k, \ldots, y_m^k)^T$ is the vector whose components are the m unknown functions ($\psi_1^k, D_1^k, \phi_{n,1}^k, J_{n,1}^k, \psi_2^k, D_2^k, \phi_{n,2}^k, J_{n,2}^k, \psi_3^k, D_3^k, \phi_{n,3}^k$, and $J_{n,3}^k$ for HBVs and, ψ^k, D^k, ϕ_n^k, and J_n^k for SBVs). The h_j values are the distances between adjacent grid points ($x_{j+1} - x_j$).

The temporally discretized boundary constraints at the boundary x_{B1},

$$G_i^k(x_{B1}, y^k(x_{B1})) = 0, \tag{A.48}$$

take on the temporally and spatially discretized form of

$$G^k_{i,1}(x_1, y^k_1) = 0 \tag{A.49}$$

where $i = 1, 2, 3, \ldots\ldots, 6$ for HBVs and $i = 1, 2$ for SBVs. Likewise, the temporally discretized boundary constraints at the boundary x_{B2},

$$G^k_i(x_{B2}, y^k(x_{B2})) = 0, \tag{A.50}$$

take on the temporally and spatially discretized form of

$$G^k_{i,N+1}(x_{N+1}, y^k_{N+1}) = 0 \tag{A.51}$$

where $i = 7, 8, 9, \ldots\ldots, 12$ for HBVs and $i = 3, 4$ for SBVs.

A.3 Coupled-Equation Newton-Raphson Solution Technique

The technique utilized to solve for the state variables at the N+1 grid points at time step k is based on the coupled-equation Newton-Raphson method, and is similar to the technique described in references [A.2] and [A.3]. The discrete system of $m \times (N+1)$ equations can be defined by the nonlinear operator $\hat{A}$

$$\hat{A}(y) = \begin{bmatrix} A_1(y) \\ A_2(y) \\ \vdots \\ A_{r+1}(y) \\ \vdots \\ A_{r+m+1}(y) \\ \vdots \\ \vdots \\ \vdots \\ A_{mN-s+1}(y) \\ \vdots \\ A_{(m-1)(N+1)}(y) \\ A_{m(N+1)}(y) \end{bmatrix} = \begin{bmatrix} G^k_{1,1} \\ G^k_{i,1} \;\; i = 2, \ldots, r \\ \vdots \\ F^k_{i,1} \;\; i = 1, 2, \ldots, m \\ \vdots \\ F^k_{i,2} \;\; i = 1, 2, \ldots, m \\ \vdots \\ \vdots \\ \vdots \\ F^k_{i,N} \;\; i = 1, 2, \ldots, m \\ \vdots \\ G^k_{i,N+1} \;\; i = 1, \ldots, s-1 \\ G^k_{s,N+1} \end{bmatrix} = 0, \quad \begin{cases} r = s = 6, \text{HBVs} \\ r = s = 2, \text{SBVs} \end{cases} . \tag{A.52}$$

The solution of this system of nonlinear equations is obtained via the Newton-Raphson method as follows:

1. Solve the linear system

$$\hat{J}(y^p)\,\Delta y^p = -\hat{A}(y^p)\,, \tag{A.53}$$

where $\hat{J}(y^p)$ is the linear Jacobian matrix at iteration p and

$$\Delta y^p = (\Delta y^p_{1,1}, \ldots, \Delta y^p_{m,1}, \Delta y^p_{1,2}, \ldots, \Delta y^p_{m,2}, \ldots, \Delta y^p_{1,N+1}, \ldots, \Delta y^p_{m,N+1})^T. \tag{A.54}$$

As discussed in *Section 2.2*, the initial solution $y^{p=0}$ is obtained from the thermal equilibrium solution for the initial time step ($k = 0$); for subsequent time steps, $y^{p=0}$ is obtained from the final solution at the previous time step.

2. Correct the previous solution

$$y^{p+1} = y^p + t^p \Delta y^p\,, \tag{A.55}$$

where t^p is a damping parameter which insures that the norm of the residual $\|\hat{A}(y^p)\|$ decreases for each iteration.

3. Iterate on 1. and 2. until convergence is obtained.

The linear Jacobian matrix $\hat{J}(y)$ is the Frechet derivative of $\hat{A}(y)$, and is given by

$$\hat{J}(y) \equiv \hat{A}'(y) = \begin{bmatrix} \frac{\partial A_1}{\partial y_{1,1}} & \cdots & \frac{\partial A_1}{\partial y_{m,1}} & \frac{\partial A_1}{\partial y_{1,2}} & \cdots & \frac{\partial A_1}{\partial y_{m,2}} & \cdots & \frac{\partial A_1}{\partial y_{1,N+1}} & \cdots & \frac{\partial A_1}{\partial y_{m,N+1}} \\ \frac{\partial A_2}{\partial y_{1,1}} & \cdots & & & & & & & & \vdots \\ \vdots & & & & & & & & & \vdots \\ \frac{\partial A_{m(N+1)}}{\partial y_{1,1}} & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \cdots & \frac{\partial A_{m(N+1)}}{\partial y_{m,N+1}} \end{bmatrix}. \tag{A.56}$$

The ordering scheme utilized in defining the nonlinear operator $\hat{A}(y)$ is such that the Jacobian matrix is in the sparse $m \times m$ block tridiagonal form

$$\hat{J}(\mathbf{y}) = \begin{bmatrix} D_1 & U_1 & 0 & \dots & \dots & \dots & \dots & \dots & \dots & 0 \\ L_2 & D_2 & U_2 & 0 & \dots & & & & & \vdots \\ 0 & L_3 & D_3 & U_3 & 0 & \dots & & & & \vdots \\ \vdots & & & & & & & & & \vdots \\ \vdots & & & & & & & & & \vdots \\ \vdots & & & & \dots & 0 & L_{N-1} & D_{N-1} & U_{N-1} & 0 \\ \vdots & & & & & \dots & 0 & L_N & D_N & U_N \\ 0 & \dots & \dots & \dots & \dots & \dots & \dots & 0 & L_{N+1} & D_{N+1} \end{bmatrix}. \qquad \text{(A.57)}$$

Finally, solution of the linear system given by equation (A.53) is accomplished via the LU decomposition of the Jacobian matrix $\hat{J}(\mathbf{y})$, and the subsequent use of the L and U matrices to calculate $\Delta\mathbf{y}^p$ by forward- and backward-substitution. A partial pivoting scheme guarantees the stable decomposition of the block tridiagonal Jacobian matrix into L and U matrices which retain the sparse block structure of $\hat{J}(\mathbf{y})$.

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Appendix B

GaAs, $Al_xGa_{1-x}As$, $In_xGa_{1-x}As$, $In_xAl_{1-x}As$, and InP Material Parameters

Relevant details about the temperature- and composition-dependent material parameters for GaAs, $Al_xGa_{1-x}As$, $In_xGa_{1-x}As$, $In_xAl_{1-x}As$, and InP have been taken from references [B.1] through [B.20], and are summarized in Table B.1 and Table B.2. Material parameters with unknown temperature variation have been assumed to be temperature-independent. Ternary compound material parameters not given in Table B.1 have been linearly interpolated between the parameters of their constituent binary materials using the parameter values given in Table B.2, as well as the following temperature-dependent parameters fit to experimental data:

$$\varepsilon_{r,\,GaAs} = 12.677 + 4.792x10^{-4}T + 4.033x10^{-6}T^2 \text{ [B.14]} \tag{B.1}$$

$$\varepsilon_{r,\,InP} = 11.817 + 1.431x10^{-3}T + 3.482x0^{-6}T^2 \text{ [B.15]} \tag{B.2}$$

$$E^{\Gamma}_{g,\,AlAs}(\text{eV}) = 3.135 - \frac{8.410x10^{-4}T^2}{T + 408.0} \text{ [B.4]} \tag{B.3}$$

$$E^{L}_{g,\,InP}(\text{eV}) = 2.040 - \frac{4.360x10^{-4}T^2}{T + 136.0} \text{ [B.3, B.16]} \tag{B.4}$$

$$E^{X}_{g,\,InP}(\text{eV}) = 2.400 - \frac{1.453x10^{-3}T^2}{T + 136.0} \text{ [B.3, B.16]} \tag{B.5}$$

$$C_{11,\,GaAs}(10^{12}\ \text{dyn}\cdot\text{cm}^{-2}) = 1.211 - \frac{3.840x10^{-4}T^2}{T + 983.7} \text{ [B.17]} \tag{B.6}$$

$$C_{12,\,GaAs}(10^{12}\ \text{dyn}\cdot\text{cm}^{-2}) = 0.548 - \frac{2.580x10^{-4}T^2}{T + 1884.5} \text{ [B.17]} \tag{B.7}$$

$$E^{\Gamma}_{g,\,GaAs}\,(\text{eV}) = 1.519 - \frac{5.405x10^{-4}T^2}{T+204.0} \quad [\text{B.1}]$$

$$E^{L}_{g,\,GaAs}\,(\text{eV}) = 1.815 - \frac{6.050x10^{-4}T^2}{T+204.0} \quad [\text{B.1}]$$

$$E^{X}_{g,\,GaAs}\,(\text{eV}) = 1.981 - \frac{4.600x10^{-4}T^2}{T+204.0} \quad [\text{B.1}]$$

$$E^{\Gamma}_{g,\,InAs}\,(\text{eV}) = 0.420 - \frac{2.500x10^{-4}T^2}{T+75.0} \quad [\text{B.2}]$$

$$E^{\Gamma}_{g,\,InP}\,(\text{eV}) = 1.432 - \frac{4.100x10^{-4}T^2}{T+136.0} \quad [\text{B.3}]$$

$$E^{\Gamma}_{g,\,Al(x)Ga(1-x)As}\,(\text{eV}) = E^{\Gamma}_{g,\,GaAs} + 1.087x + 0.438x^2 \quad [\text{B.4}]$$

$$E^{X}_{g,\,Al(x)Ga(1-x)As}\,(\text{eV}) = E^{X}_{g,\,GaAs} + 0.100x + 0.160x^2 \quad [\text{B.4}]$$

$$E^{L}_{g,\,Al(x)Ga(1-x)As}\,(\text{eV}) = E^{L}_{g,\,GaAs} + 0.695x \quad [\text{B.4}]$$

$$E_{g,\,Al(x)Ga(1-x)As}\,(\text{eV}) = min\,(E^{\Gamma}_{g,\,Al(x)Ga(1-x)As},\, E^{L}_{g,\,Al(x)Ga(1-x)As},\, E^{X}_{g,\,Al(x)Ga(1-x)As})$$

$$E^{\Gamma}_{g,\,In(x)Ga(1-x)As}\,(\text{eV}) = E^{\Gamma}_{g,\,GaAs} + (E^{\Gamma}_{g,\,InAs} - E^{\Gamma}_{g,\,GaAs})\,x + \gamma_{In(x)Ga(1-x)As}x^2 + \Delta E_{g,\,strain}$$

$$E^{\Gamma}_{g,\,In(x)Al(1-x)As}\,(\text{eV}) = E^{\Gamma}_{g,\,AlAs} + (E^{\Gamma}_{g,\,InAs} - E^{\Gamma}_{g,\,AlAs})\,x + \gamma_{In(x)Al(1-x)As}x^2 + \Delta E_{g,\,strain}$$

$$\gamma_{In(x)Ga(1-x)As} = \begin{cases} 6.8840x10^{-4}T + 0.4970, & T < 77\ \text{K} \\ -4.9750x10^{-4}T + 0.5883, & T \geq 77\ \text{K} \end{cases} \qquad \gamma_{In(x)Al(1-x)As} = -3.3125x10^{-4}T + 0.8633$$

$$(\chi_{GaAs} - \chi_{Al(x)Ga(1-x)As})\,(\text{eV}) = \Delta E_g - \Delta E_v = E_{g,\,Al(x)Ga(1-x)As} - E^{\Gamma}_{g,\,GaAs} - \Delta E_{v,\,Al(x)Ga(1-x)As/GaAs}$$

$$(\chi_{GaAs} - \chi_{In(x)Ga(1-x)As})\,(\text{eV}) = (E^{\Gamma}_{g,\,In(x)Ga(1-x)As} - E^{\Gamma}_{g,\,GaAs})\left(\frac{\Delta E_c}{\Delta E_g}\right)_{GaAs/In(x)Ga(1-x)As}$$

$$(\chi_{InP} - \chi_{In(x)Ga(1-x)As})\,(\text{eV}) = (E^{\Gamma}_{g,\,In(x)Ga(1-x)As} - E^{\Gamma}_{g,\,InP})\left(\frac{\Delta E_c}{\Delta E_g}\right)_{InP/In(x)Ga(1-x)As}$$

$$(\chi_{InP} - \chi_{In(x)Al(1-x)As})\,(\text{eV}) = E^{\Gamma}_{g,\,In(x)Al(1-x)As} - E^{\Gamma}_{g,\,InP} + \Delta E_{v,\,InP/In(x)Al(1-x)As}$$

$$\frac{m^*_{\Gamma,\,GaAs}}{m^*_o} = 0.067 - \left(\frac{0.004}{300}\right)T \quad [\text{B.1}]$$

$$\frac{m^*_{\Gamma,\,InP}}{m^*_0} = 0.082 - \left(\frac{0.006}{300}\right)T \quad [\text{B.5}]$$

$$N^{\Gamma,L,X}_c\,(\text{cm}^{-3}) = 2\left[\frac{2\pi m^*_{\Gamma,L,X}kT}{h^2}\right]^{3/2}$$

$$N_v\,(\text{cm}^{-3}) = 2\left[\frac{2\pi kT}{h^2}\right]^{3/2}[\,(m^*_{hh})^{3/2} + (m^*_{lh})^{3/2}]$$

$$N_c\,(\text{cm}^{-3}) = N^{\Gamma}_c\,\exp\left(\frac{E_{g,\,min} - E^{\Gamma}_g}{kT}\right) + N^{L}_c\,\exp\left(\frac{E_{g,\,min} - E^{L}_g}{kT}\right) + N^{X}_c\,\exp\left(\frac{E_{g,\,min} - E^{X}_g}{kT}\right)$$

$$n_{i,\,ref}\,(\text{cm}^{-3}) = \sqrt{N_{v,\,ref}\,N^{\Gamma}_{c,\,ref}}\,\exp\left(\frac{-E_{g,\,ref}}{2kT}\right)$$

Table B.1 Energy band structure and carrier statistics material parameters for GaAs, $Al_xGa_{1-x}As$, $In_xGa_{1-x}As$, $In_xAl_{1-x}As$, and InP.

Table B.2 Material parameters for AlAs, GaAs, InAs, and InP.

	Material			
Parameter	**AlAs**	**GaAs**	**InAs**	**InP**
a (Å)	5.6611[B.6]	5.6533[B.6]	6.0584[B.7]	5.8688[B.7]
ε_r	10.06[B.6]	see Eqn. (B.1)	14.55[B.8]	see Eqn. (B.2)
$m^*_{\Gamma,\,DS}/m_0$	0.150[B.6]	see Table B.1	0.023[B.7]	see Table B.1
$m^*_{L,\,DS}/m_0$	0.660[B.6]	0.560[B.6]	—	0.655[B.9]
$m^*_{X,\,DS}/m_0$	0.710[B.6]	0.850[B.6]	—	0.676[B.9]
m^*_{hh}/m_0	0.760[B.6]	0.480[B.10]	0.600[B.7]	0.560[B.11]
m^*_{lh}/m_0	0.150[B.6]	0.087[B.10]	0.027[B.7]	0.120[B.11]
b (eV)	-1.5[B.6]	-1.7[B.6]	-1.8[B.7]	—
$(\partial E_g/\partial P)_T$ (10^{-12} eV·cm^2/dyn)	10.2[B.6]	11.5[B.12]	10.0[B.12]	—
C_{11} (10^{12} dyn/cm^2)	1.202[B.6]	see Eqn. (B.6)	see Eqn. (B.8)	—
C_{12} (10^{12} dyn/cm^2)	0.570[B.6]	see Eqn. (B.7)	see Eqn. (B.9)	—
χ (eV)	—	4.07[B.13]	—	4.38[B.13]

$$C_{11,\,InAs}\,(10^{12}\ \text{dyn}\cdot\text{cm}^{-2}) = 0.883 - 1.890x10^{-4}T \text{ [B.18]} \tag{B.8}$$

$$C_{12,\,InAs}\,(10^{12}\ \text{dyn}\cdot\text{cm}^{-2}) = 0.508 - 1.840x10^{-4}T \text{ [B.18].} \tag{B.9}$$

For GaAs/$In_xGa_{1-x}As$/$Al_xGa_{1-x}As$ devices, it is important to note that only the central (Γ) valley contribution to the density of states in GaAs has been utilized. This insures that the density of states in GaAs matches the density of states in $In_xGa_{1-x}As$, graded to a composition of zero, on GaAs since details about the high energy bandstructure of $In_xGa_{1-x}As$ on GaAs are not well established.

The unstrained energy gaps of both $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ have been obtained using energy gap values for the constituent binary compounds as well as energy gap values for $In_xGa_{1-x}As$[B.19] and $In_xAl_{1-x}As$[B.20] lattice-matched to InP. The temperature dependence of these energy gaps has been modeled by allowing the bowing parameters, γ_{InGaAs} and γ_{InAlAs}, to vary with temperature. All lattice-mismatched layers are assumed to be coherently strained. As such, strain corrections to the energy gaps of (100)-oriented pseudomorphic $In_xGa_{1-x}As$ and $In_xAl_{1-x}As$ layers have been modeled as[B.21]

$$\Delta E_{g,\,strain}\,(eV) = \left(\frac{C_{11}+2C_{12}}{C_{11}}\right)\left[\frac{2}{3}(C_{12}-C_{11})\left(\frac{\partial E_g}{\partial P}\right)_T - b\right]\left(\frac{a_s-a}{a}\right) \tag{B.10}$$

where a_s is the substrate (GaAs or InP) lattice constant and a is the unstrained lattice constant of the appropriate heteroepitaxial layer ($In_xGa_{1-x}As$ or $In_xAl_{1-x}As$); the C_{ij} are elastic stiffness constants, $(\partial E_g/\partial P)_T$ is the bandgap pressure coefficient at a constant temperature, and b is the valence-band deformation potential, each for the appropriate heteroepitaxial layer ($In_xGa_{1-x}As$ or $In_xAl_{1-x}As$). Finally, modified electron affinities (see Table B.1) have been utilized, based on recent experimental studies, to provide correct bandgap discontinuities; modified electron affinities have also been utilized to provide correct metal-semiconductor interface barrier heights (see equation (2.23)). The conduction- and valence-band discontinuity factors utilized for this work are given in Table B.3 along with the resulting heterointerface barrier heights for several important heterojunctions.

Table B.3 Conduction- and valance-band discontinuity factors and the resulting heterointerface barrier heights for several important heterojunctions.

$\Delta E_{v,Al(x)Ga(1-x)As/GaAs}$ (eV)	$0.53x$[a]
$(\Delta E_c/\Delta E_g)_{GaAs/In(x)Ga(1-x)As}$	0.55[B.22]
$(\Delta E_c/\Delta E_g)_{InP/In(x)Ga(1-x)As}$	0.43[B.23]
$\Delta E_{v,InP/In(x)Al(1-x)As}$ (eV)	$-0.27+0.73x+0.1864x^2$[B.24]
$\Delta E_{c,Al(0.4)Ga(0.6)As/GaAs} = 293$ meV	
$\Delta E_{c,Al(0.7)Ga(0.7)As/GaAs} = 254$ meV	
$\Delta E_{c,Al(0.4)Ga(0.6)As/In(0.2)Ga(0.8)As} = 407$ meV	
$\Delta E_{c,Al(0.7)Ga(0.3)As/In(0.2)Ga(0.8)As} = 368$ meV	
$\Delta E_{c,In(0.53)Ga(0.47)As/InP} = 258$ meV	
$\Delta E_{c,In(0.52)Al(0.48)As/In(0.53)Ga(0.47)As} = 515$ meV	

a. This valence-band offset is a compromise between the values recommended in references [B.25] and [B.26].

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Appendix C

The Accelerated Fixed-Point Harmonic-Balance Circuit Analysis Technique

At the heart of the Accelerated Fixed-Point (AFP) harmonic-balance circuit analysis technique[C.1] of Chapter 3 is the voltage update expression of equation (3.1). A detailed derivation of this equation is presented in this appendix.

C.1 The Multiple-Reflection Algorithm in Fixed-Point Iterative Form

As noted in Chapter 3, the AFP harmonic-balance circuit analysis method is based on the Multiple-Reflection (MR) algorithm[C.2, C.3]. The key to deriving the voltage update expression at the heart of the AFP harmonic-balance method is formulating the MR algorithm as a fixed-point iterative scheme. In this form, the MR algorithm explicitly expresses the new harmonic voltage component, $V_{n,k+1}$, at the terminals of the intrinsic nonlinear device as a nonlinear mapping of the previous harmonic voltage component, $V_{n,k}$, and the previous harmonic current component, $I_{n,k}$.

The circuit partitioning scheme for the MR algorithm, shown schematically in Figure C.1, is characterized by the insertion of a set of fictitious lossless transmission lines between the respective ports of the linear and nonlinear subcircuits. By making the transmission lines an integral number of wavelengths long at the fundamental frequency, and hence at the harmonics of the fundamental frequency, the steady-state waves of the modified circuit will be the same as those of the original circuit, that is the harmonic currents as well as the harmonic voltages at the two ends of the transmission lines (the ports of the linear and nonlinear subcircuits) will be the same. By making the transmission lines electrically long, this partitioning scheme separates the nonlinear circuit analysis into two alternating *steady-state* analyses, one between the linear subcircuit and the transmission lines in the frequency-domain, and one between the nonlinear subcircuit and the

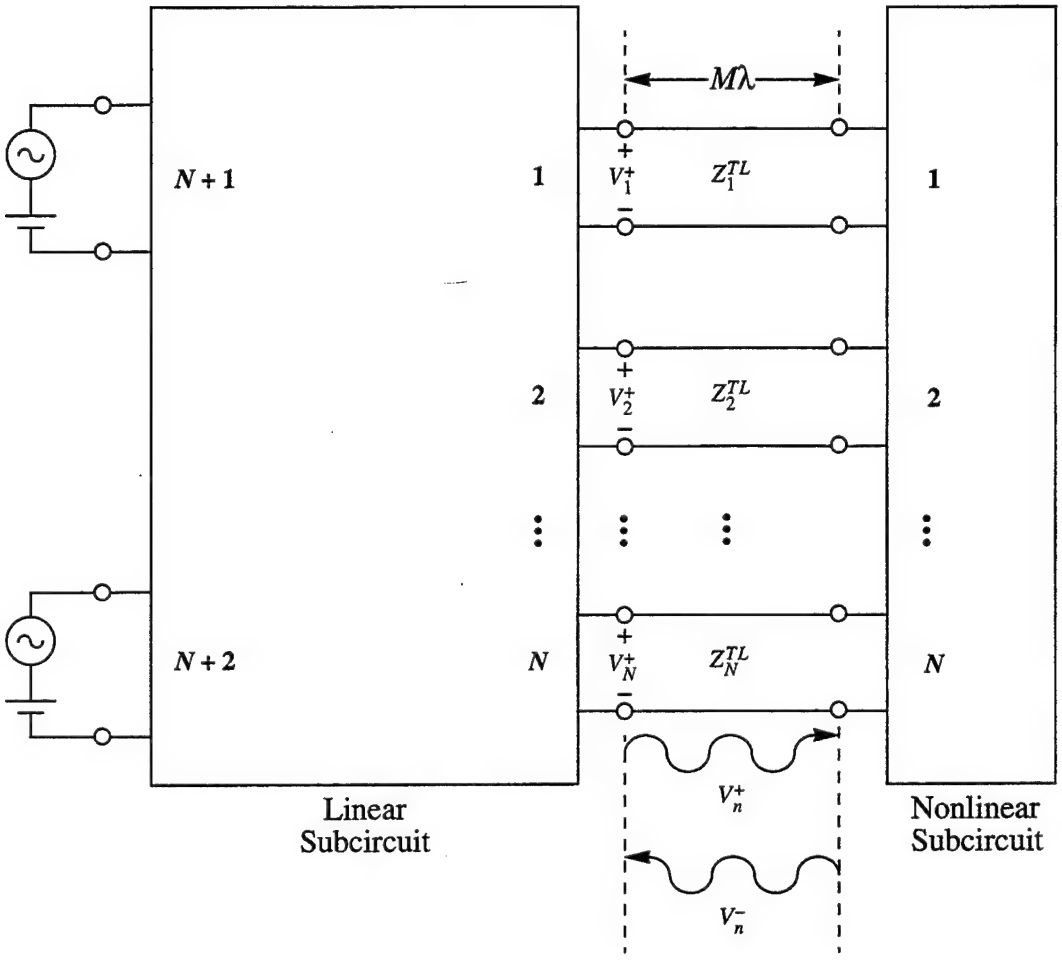

Figure C.1 Generalized partitioning scheme for separating the a nonlinear two-port component into linear and nonlinear subcircuits using fictitious ideal and electrically long transmission lines for analysis via the MR algorithm.

transmission lines in the time-domain. Furthermore, this partitioning scheme allows for the use of incident (positive-travelling, V^+) and reflected (negative-travelling, V^-) harmonic voltages waves, composed of linear combinations of the total harmonic voltages and currents at the terminals of the nonlinear subcircuit, as the state variables in the nonlinear circuit analysis. As such, the spatially varying total instantaneous voltage on the transmission line at harmonic n is the sum of the positive- and negative-travelling voltage waves

$$V_n(x) = V_n^+(x) + V_n^-(x) . \tag{C.1}$$

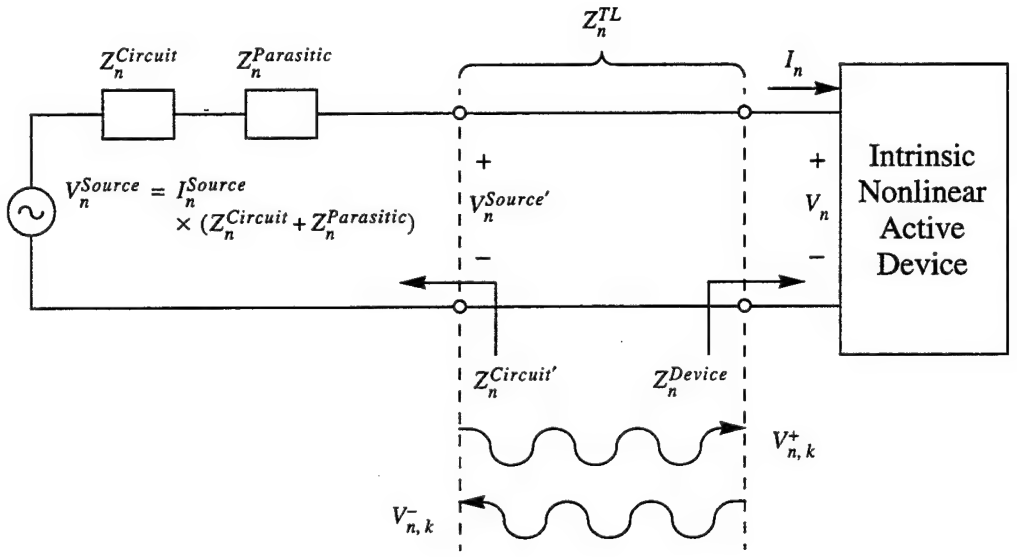

Figure C.2 Schematic representation of a frequency multiplier circuit used for the derivation of the AFP harmonic-balance voltage update expression.

Likewise, the spatially varying total instantaneous current on the transmission line at harmonic n is the difference between the positive- and negative-travelling current waves

$$I_n(x) = I_n^+(x) - I_n^-(x) \tag{C.2}$$

which can be rewritten in terms of the positive- and negative-travelling voltage waves as

$$I_n(x) = \frac{V_n^+(x) - V_n^-(x)}{Z_n^{TL}}. \tag{C.3}$$

With this partitioning scheme in mind, the MR algorithm can be formulated as a fixed-point iterative method; the derivation to follow is based on the frequency multiplier circuit of Figure C.2. The total voltage at the terminals of the intrinsic active device, $V_{n,k+1}$, for harmonic n and iteration $k+1$ is the sum of the positive- and negative-travelling harmonic voltage waves on the fictitious transmission line, and can be expressed as a function of the positive-travelling harmonic voltage wave and the reflection coefficient of the intrinsic active device by

$$V_{n,k+1} = (1 + \rho_{n,k}^{Device})\, V_{n,k}^{+} \tag{C.4}$$

where the harmonic reflection coefficient of the intrinsic device is given by

$$\rho_{n,k}^{Device} = \frac{Z_{n,k}^{Device} - Z_n^{TL}}{Z_{n,k}^{Device} + Z_n^{TL}} \tag{C.5}$$

and

$$1 + \rho_{n,k}^{Device} = \frac{2Z_{n,k}^{Device}}{Z_{n,k}^{Device} + Z_n^{TL}}. \tag{C.6}$$

Since the harmonic impedance of the intrinsic device ($Z_{n,k}^{Device} = V_{n,k}/I_{n,k}$) changes with each iteration k, the harmonic reflection coefficient of the device also changes with each iteration until convergence is achieved.

The positive-travelling harmonic voltage wave, $V_{n,k}^{+}$, can be expressed as the sum of the harmonic source voltage at the terminals of the fictitious transmission line ($V_n^{Source'}$) and the negative-travelling voltage wave reflected off of the linear subcircuit,

$$V_{n,k}^{+} = V_n^{Source'} + \rho_n^{Linear} V_{n,k}^{-}, \tag{C.7}$$

where the harmonic reflection coefficient of the linear subcircuit is given by

$$\rho_n^{Linear} = \frac{Z_n^{Linear} - Z_n^{TL}}{Z_n^{Linear} + Z_n^{TL}}, \tag{C.8}$$

$$V_n^{Source'} = \frac{Z_n^{TL}}{Z_n^{TL} + Z_n^{Linear}} V_n^{Source}, \tag{C.9}$$

and

$$Z_n^{Linear} = Z_n^{Circuit} + Z_n^{Parasitic}. \tag{C.10}$$

Equation (C.7) is obtained by (1) considering the active device as the origin of the negative-travelling voltage wave, and (2) only updating the iteration number k when the positive-travelling wave reaches the terminals of the intrinsic device.

By combining equations (C.1) and (C.3), the negative-travelling harmonic voltage wave, $V_{n,k}^{-}$, can be expressed in terms of the total harmonic voltage wave, the total harmonic current wave, and the characteristic impedance of the fictitious transmission line as

$$V_{n,k}^{-} = \frac{1}{2}(V_{n,k} - Z_n^{TL} I_{n,k}) . \tag{C.11}$$

Finally, by combining equations (C.4), (C.7), and (C.11), the MR algorithm can be expressed in fixed-point iterative form as

$$V_{n,k+1} = (1 + \rho_{n,k}^{Device}) \left[V_n^{Source'} + \frac{1}{2} \rho_n^{Linear} (V_{n,k} - Z_n^{TL} I_{n,k}) \right] . \tag{C.12}$$

Again, this equation explicitly expresses the new harmonic voltage component, $V_{n,k+1}$, at the terminals of the intrinsic nonlinear device as a nonlinear mapping of the previous harmonic voltage component, $V_{n,k}$, and the previous harmonic current component, $I_{n,k}$. Equation (C.12) can be rewritten, using equations (C.6), (C.8), and (C.9), as

$$V_{n,k+1} = \frac{2Z_{n,k}^{Device}}{Z_{n,k}^{Device} + Z_n^{TL}} \frac{Z_n^{TL}}{Z_n^{Linear} + Z_n^{TL}} V_n^{Source} + \frac{Z_n^{Linear} - Z_n^{TL}}{Z_n^{Linear} + Z_n^{TL}} \frac{2Z_{n,k}^{Device}}{Z_{n,k}^{Device} + Z_n^{TL}} \frac{1}{2}(V_{n,k} - Z_n^{TL} I_{n,k}) \tag{C.13}$$

which is the same as equation (1) of reference [C.1]. It is important to note that at convergence to the steady-state ($k \to \infty$), $V_{n,k+1} = V_{n,k} = V_n$ and equations (C.12) and (C.13) satisfy Kirchhoff's voltage law such that

$$V_n^{Source} = V_n + Z_n^{Linear} I_n . \tag{C.14}$$

C.2 The Accelerated Fixed-Point Harmonic-Balance Voltage Update Expression

The voltage update expression central to the AFP harmonic-balance method can be derived from equation (C.13) in a straight-forward manner. For undriven harmonics, $V_n^{Source} = 0$ and the steady-state solution is known *a priori*, from Kirchhoff's voltage law, to be

$$Z_n^{Device} = -Z_n^{Linear}. \tag{C.15}$$

Using these simplification in equation (C.13) yields

$$V_{n,k+1} = \frac{Z_n^{Linear}}{Z_n^{Linear} + Z_n^{TL}} \left(V_{n,k} - Z_n^{TL} I_{n,k}\right). \tag{C.16}$$

For the driven harmonics, the source term V_n^{Source} is incorporated into equation (C.16) such that Kirchhoff's voltage law is preserved at convergence to the steady-state. This yields the general AFP harmonic-balance voltage update expression

$$V_{n,k+1} = \frac{Z_n^{TL}}{Z_n^{Linear} + Z_n^{TL}} V_n^{Source} + \frac{Z_n^{Linear}}{Z_n^{Linear} + Z_n^{TL}} \left(V_{n,k} - Z_n^{TL} I_{n,k}\right) \tag{C.17}$$

outlined in Chapter 3 (see equation (3.1)). Again, it is important to note that at convergence to the steady-state $(k \to \infty)$, $V_{n,k+1} = V_{n,k} = V_n$ and equation (C.17) satisfies Kirchhoff's voltage law such that

$$V_n^{Source} = V_n + Z_n^{Linear} I_n. \tag{C.18}$$

Appendix C References

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[C.2] A. R. Kerr, "A Technique for Determining the Local Oscillator Waveforms in a Microwave Mixer," *IEEE Trans. Microwave Theory Tech.*, Vol. 23, No. 10, October 1975, pp. 66-69.

[C.3] P. H. Siegel, A. R. Kerr, and W. Hwang, "Topics in the Optimization of Millimeter-wave Mixers," *NASA Tech. Papers*, No. 2287, March 1984.

Appendix D

D.C. and Frequency-Dependent Parasitic Impedances of Whisker-Contacted and Planar Geometry Diodes

This appendix catalogs the d.c. and frequency-dependent parasitic impedances of Heterostructure Barrier Varactor (HBV) and Schottky Barrier Varactor (SBV) frequency multiplier devices required for the nonlinear circuit simulation technique of Chapter 3. Parasitic impedances for whisker-contacted geometry HBV and SBV frequency multiplier devices as well as planar geometry HBV frequency multiplier devices are given. In the expressions presented below, t signifies a generic thickness, w a width, and l a length.

D.1 Parasitic Impedances of Whisker-Contacted Geometry Frequency Multiplier Devices

D.1.1 D.C. Parasitic Impedances

The d.c. parasitic impedances of a whisker-contacted geometry HBV frequency multiplier device are given, in reference to Figure D.1, by

$$R_{oc\_anode} = \frac{\rho_{oc\_anode}}{\pi r_{anode}^2}, \tag{D.1}$$

$$R_{mesa\_epi1} = \frac{t_{mesa\_epi1}}{\sigma_{dc,\,epi1}\pi r_{anode}^2}, \tag{D.2}$$

$$R_{mesa\_epi2} = \frac{t_{mesa\_epi2}}{\sigma_{dc,\,epi2}\pi r_{anode}^2}, \tag{D.3}$$

$$R_{mesa\_substrate} = \frac{t_{mesa\_substrate}}{\sigma_{dc,\,substrate}\pi r_{anode}^2}, \tag{D.4}$$

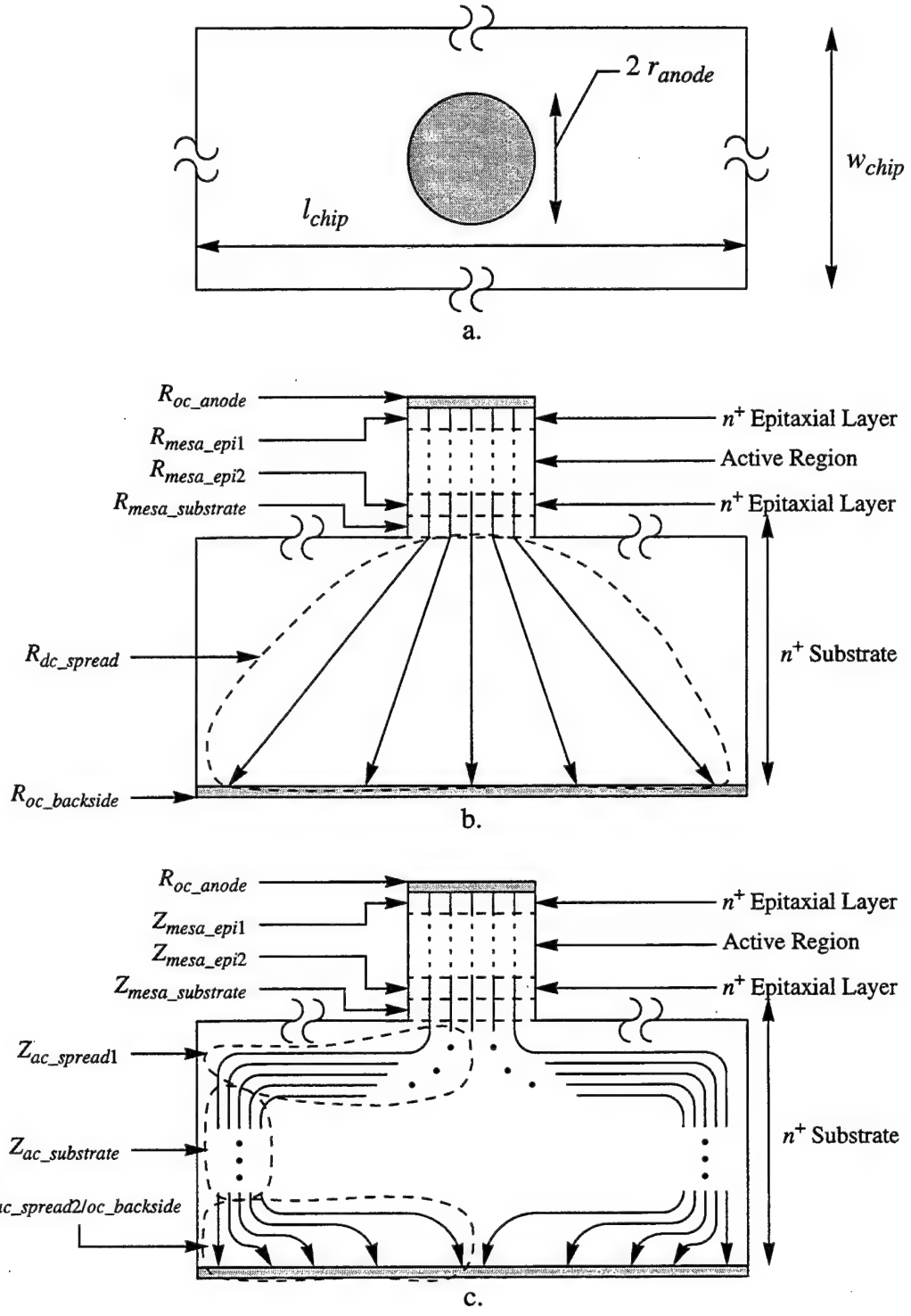

Figure D.1 Top (a.) and cross-sectional (b. and c.) views of a whisker-contacted geometry HBV frequency multiplier showing the d.c. (b.) and frequency-dependent (c.) parasitic impedances. For SBVs, the parasitic impedances associated with the mesa and anode ohmic contact are neglected.

$$R_{dc\_spread} = \frac{1}{4\sigma_{dc,\,substrate} r_{anode}} \text{ [D.1, D.2]}, \tag{D.5}$$

and

$$R_{oc\_backside} = \frac{\rho_{oc\_backside}}{l_{chip} w_{chip}}, \tag{D.6}$$

where, in generic terms, the d.c. material conductivity is

$$\sigma_{dc} = q\mu_n N_D . \tag{D.7}$$

D.1.2 Frequency-Dependent Parasitic Impedances

The frequency-dependent parasitic impedances of a whisker-contacted geometry HBV frequency multiplier device are given, in reference to Figure D.1, by

$$R_{oc\_anode} = \frac{\rho_{oc\_anode}}{\pi r_{anode}^2}, \tag{D.8}$$

$$Z_{mesa\_epi1} = \frac{t_{mesa\_epi1}}{\sigma_{ac,\,epi1} \pi r_{anode}^2}, \tag{D.9}$$

$$Z_{mesa\_epi2} = \frac{t_{mesa\_epi2}}{\sigma_{ac,\,epi2} \pi r_{anode}^2}, \tag{D.10}$$

$$Z_{mesa\_substrate} = \frac{t_{mesa\_substrate}}{\sigma_{ac,\,substrate} \pi r_{anode}^2}, \tag{D.11}$$

$$R_{ac\_spread1} = \frac{\omega\mu_0 r_{anode}}{2\pi}\left\{\frac{\varsigma_2}{|\varsigma|^2}\left[\ln\left(\frac{r_{equiv.\_chip\_area}}{r_{anode}}\right)+\ln(|\varsigma|)+C-1\right]\right.$$
$$-\frac{\varsigma_1}{|\varsigma|^2}\operatorname{asinh}\left(\frac{\varsigma_2}{|\varsigma|}\right)$$
$$\left.+\frac{\pi\varsigma_1\varsigma_2}{|\varsigma|^4}-\frac{5}{36}\varsigma_2+\frac{\pi}{45}\varsigma_1\varsigma_2-\frac{269}{7200}\varsigma_1^2\varsigma_2+\frac{269}{21600}\varsigma_2^3+\frac{4\pi}{945}\varsigma_1\varsigma_2(\varsigma_1^2-\varsigma_2^2)\right\} \quad [D.2], \quad (D.12)$$

$$X_{ac\_spread1} = \frac{\omega\mu_0 r_{anode}}{2\pi}\left\{\frac{\varsigma_1}{|\varsigma|^2}\left[\ln\left(\frac{r_{equiv.\_chip\_area}}{r_{anode}}\right)+\ln(|\varsigma|)+C-1\right]\right.$$
$$+\frac{\varsigma_2}{|\varsigma|^2}\operatorname{asinh}\left(\frac{\varsigma_2}{|\varsigma|}\right)+\frac{\pi(\varsigma_1^2-\varsigma_2^2)^2}{2|\varsigma|^4}-\frac{\pi}{6}+\frac{5}{36}\varsigma_1+\frac{\pi}{90}(\varsigma_1^2-\varsigma_2^2)^2-\frac{269}{7200}\varsigma_1\varsigma_2^2$$
$$\left.+\frac{269}{21600}\varsigma_1^3+\frac{\pi}{945}\left(6\varsigma_1^2\varsigma_2^2-\varsigma_1^4-\varsigma_2^4\right)\right\} \quad [D.2], \quad (D.13)$$

$$Z_{ac\_spread1} = R_{ac\_spread1} + jX_{ac\_spread1} \quad (D.14)$$

$$Z_{ac\_substrate} = \frac{t_{substrate}}{2\pi r_{equiv.\_chip\_circum.}\sigma_{ac\_substrate}\delta_{skin}} \quad [D.3], \quad (D.15)$$

and

$$Z_{ac\_spread2/oc\_backside} = \frac{\beta\rho_{oc\_backside} I_0(\beta r_{equiv.\_chip\_area})}{2\pi r_{equiv.\_chip\_area} I_1(\beta r_{equiv.\_chip\_area})} \quad [D.4], \quad (D.16)$$

where C is Euler's constant, $\varsigma = \gamma r_{anode}$, $\varsigma_1 = Re\{\varsigma\}$, $\varsigma_2 = Im\{\varsigma\}$, and

$$\beta = \sqrt{\frac{1}{\sigma_{dc\_substrate}\rho_{oc\_backside}\delta_{skin}}}. \quad (D.17)$$

In generic terms and following references [D.5] and [D.6], the frequency-dependent material conductivity is

$$\sigma_{ac} = \sigma_{dc}\left[\frac{1}{1+j\left(\frac{\omega}{\omega_s}\right)}+j\left(\frac{\omega}{\omega_d}\right)\right], \tag{D.18}$$

where the scattering frequency of the material is

$$\omega_s = \frac{1}{\tau_p} = \frac{q}{m^*\mu_n}, \tag{D.19}$$

the dielectric relaxation frequency of the material is

$$\omega_d = \frac{\sigma_{dc}}{\varepsilon}, \tag{D.20}$$

the material's skin depth is

$$\delta_{skin} = \sqrt{\frac{2}{\omega\mu_0\sigma_{dc}}}, \tag{D.21}$$

and the material's propagation constant is

$$\gamma = \frac{(1+j)}{\delta_{skin}}\sqrt{\frac{1}{1+j\left(\frac{\omega}{\omega_s}\right)}+j\left(\frac{\omega}{\omega_d}\right)}. \tag{D.22}$$

For both the d.c. and frequency-dependent parasitic impedance equations, ω, μ_0, ε, q, m^*, μ_n, τ_p, and ρ_{oc} are the radian frequency of interest, the permeability of free space, the dielectric permittivity of the material, the electron charge, the electron effective mass, the electron mobility, the electron momentum relaxation time, and the specific contact resistivity of an ohmic contact, respectively. For the impedance calculations involving the substrate, a circular geometry, equivalent to the rectangular geometry of the actual chip, is assumed. As such, the radius $r_{equiv.\_chip\_area}$ is the radius of a circle having an area equivalent to that of the rectangular chip face (l_{chip} x w_{chip}) of Figure D.1. Likewise, the

radius $r_{equiv.\_chip\_circum}$ is the radius of a circle having a circumference equivalent to that of the rectangular chip face ($2l_{chip} + 2w_{chip}$) of Figure D.1.

Overall, the parasitic impedances utilized here for whisker-contacted frequency multiplier devices differ from those of references [D.3] and [D.7] as follows: (1) the result of references [D.1] and [D.2] for the purely resistive d.c. parasitic spreading impedance is used (see equation (D.5)), (2) the displacement current and mass-inertial contributions to the parasitic impedances from reference [D.6] are used (see equations (D.18)-(D.20)), (3) the spreading impedance at the backside ohmic contact as calculated in reference [D.4] is included (see equation (D.16)), and (4) the a.c. spreading impedance expressions given in reference [D.2] are used (see equations (D.12)-(D.14)).

Finally, the parasitic impedances listed above for HBVs include parasitic impedance components not required for SBVs since SBVs have much simpler, non-mesa geometries. Consequently, it is necessary to neglect the parasitic impedances associated with the anode ohmic contact (R_{oc_anode}) and mesa (R_{mesa_epi1}, R_{mesa_epi2}, R_{mesa_sub}, Z_{mesa_epi1}, Z_{mesa_epi2} and Z_{mesa_sub}) when analyzing SBVs. It is important to note, as well, that the parasitic impedances associated with these mesas neglect the skin effect since the HBV mesas typically have very small radii (on the order of 1 μm to 10 μm).

D.2 Parasitic Impedances of Planar Geometry Frequency Multiplier Devices

D.2.1 D.C. Parasitic Impedances

The d.c. parasitic impedances of a planar geometry HBV frequency multiplier device are given, in reference to Figure D.2, by

$$R_{oc\_anode} = \frac{2\rho_{oc\_anode}}{\pi r_{anode}^2}, \tag{D.23}$$

$$R_{mesa\_epi1} = \frac{2t_{mesa\_epi1}}{\sigma_{dc,\,epi1}\pi r_{anode}^2}, \tag{D.24}$$

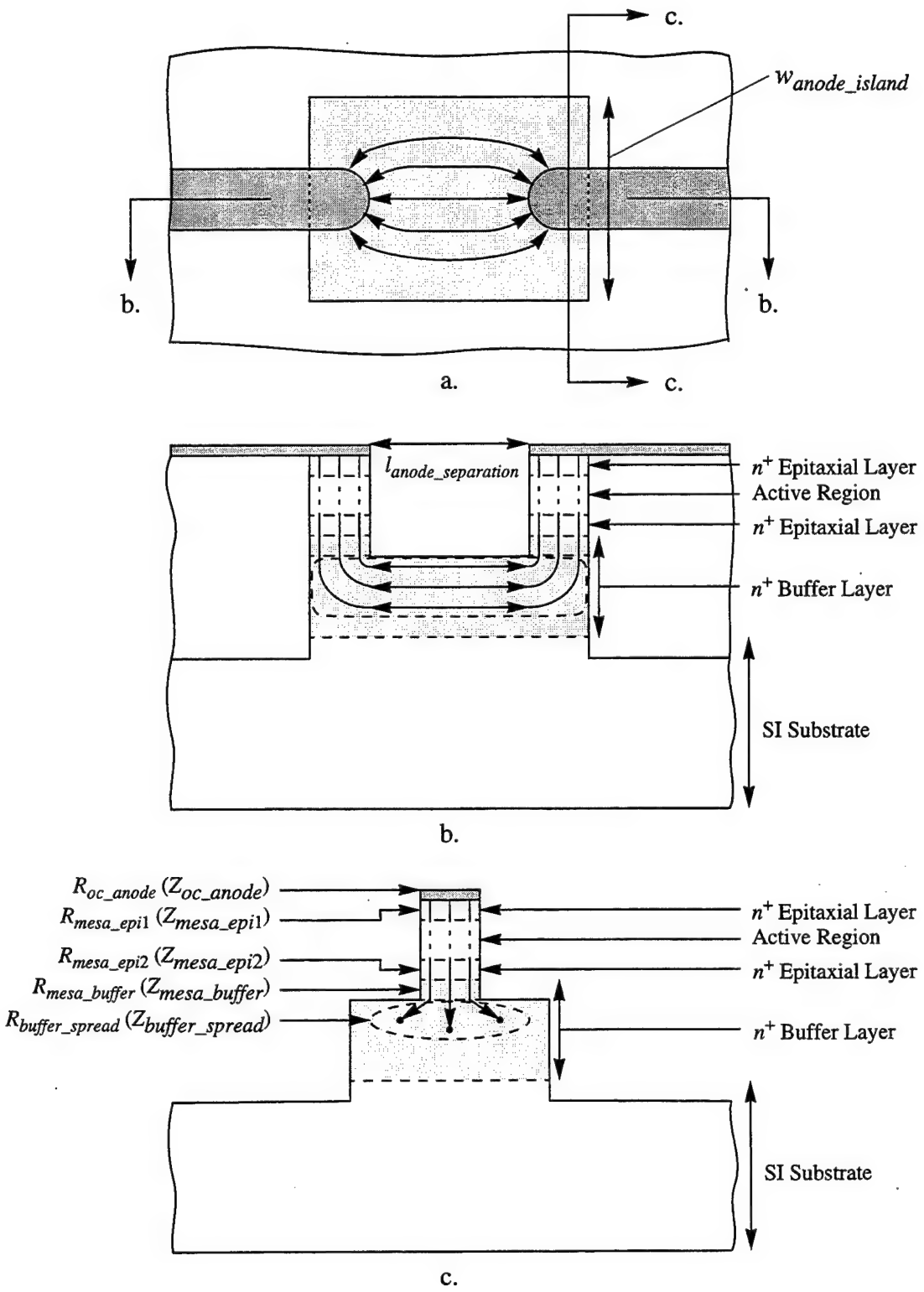

Figure D.2 Top (a.), side cross-sectional (b.), and end cross-sectional (c.) views of a planar geometry HBV frequency multiplier showing the d.c. (frequency-dependent) parasitic impedances.

$$R_{mesa\_epi2} = \frac{2t_{mesa\_epi2}}{\sigma_{dc,\,epi2}\pi r_{anode}^2}, \tag{D.25}$$

$$R_{mesa\_buffer} = \frac{2t_{mesa\_buffer}}{\sigma_{dc,\,buffer}\pi r_{anode}^2}, \tag{D.26}$$

and

$$R_{buffer\_spread} = \frac{2\left[\frac{1}{2}(t_{buffer} - t_{mesa\_buffer}) + r_{anode} + \frac{1}{2}l_{anode\_separation}\right]}{\sigma_{dc,\,buffer}\frac{1}{2}\left[\pi r_{anode}^2 + (t_{buffer} - t_{mesa\_buffer})\,w_{anode\_island}\right]}. \tag{D.27}$$

D.2.2 Frequency-Dependent Parasitic Impedances

The frequency-dependent parasitic impedances of a planar geometry HBV frequency multiplier device are given, in reference to Figure D.2, by

$$R_{oc\_anode} = \frac{2\rho_{oc\_anode}}{\pi r_{anode}^2}, \tag{D.28}$$

$$Z_{mesa\_epi1} = \frac{2t_{mesa\_epi1}}{\sigma_{ac,\,epi1}\pi r_{anode}^2}, \tag{D.29}$$

$$Z_{mesa\_epi2} = \frac{2t_{mesa\_epi2}}{\sigma_{ac,\,epi2}\pi r_{anode}^2}, \tag{D.30}$$

$$Z_{mesa\_buffer} = \frac{2t_{mesa\_buffer}}{\sigma_{ac,\,buffer}\pi r_{anode}^2}, \tag{D.31}$$

and

$$Z_{buffer\_spread} = \frac{2\left[\frac{1}{2}(t_{buffer} - t_{mesa\_buffer}) + r_{anode} + \frac{1}{2}l_{anode\_separation}\right]}{\sigma_{ac,\,buffer}\frac{1}{2}\left[\pi r_{anode}^2 + (t_{buffer} - t_{mesa\_buffer})\,w_{anode\_island}\right]}. \tag{D.32}$$

Appendix D References

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[D.2] U. V. Bhapkar, "An Investigation of the Series Impedance of GaAs Schottky Barrier Diodes," M.S.E.E. Thesis, University of Virginia, May 1990, pp. 25-28 and 31-34.

[D.3] P. H. Siegel, A. R. Kerr, and W. Hwang, "Topics in the Optimization of Millimeter-wave Mixers," *NASA Tech. Papers*, No. 2287, March 1984.

[D.4] J. A. Calviello, J. L. Wallace, and P. R. Bie, "High Performance GaAs Quasi-Planar Varactors for Millimeter Waves," *IEEE Trans. Electron Dev.*, Vol. 21, No. 10, October 1974, pp. 624-630.

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Appendix E

Thermal Resistances of Heterostructure Barrier Varactor Frequency Multiplier Circuit Constituent Elements

This appendix catalogs the thermal resistance expressions for Heterostructure Barrier Varactors (HBVs) that were used to calculate the HBV thermal properties presented in Chapter 4; thermal resistance expressions for both whisker-contacted and planar geometry HBV frequency multiplier circuits are given. In the expressions presented below, t signifies a generic thickness, w a width, and l a length.

E.1 Thermal Resistances of Whisker-Contacted Geometry HBV Frequency Multiplier Circuits

The thermal resistance expressions for whisker-contacted geometry HBV frequency multiplier circuits are given, in reference to Figures E.1 and E.2, by:

$$R_{active,\,half1} = \frac{\frac{1}{2}t_{active}}{\kappa_{GaAs}\left(N_{D,\,active}, \frac{1}{2}(T_{-3}+T_{-4})\right)\pi r_{anode}^2} \tag{E.1}$$

$$R_{nplus1} = \frac{t_{nplus1}}{\kappa_{GaAs}\left(N_{D,\,nplus1}, \frac{1}{2}(T_{-2}+T_{-3})\right)\pi r_{anode}^2} \tag{E.2}$$

$$R_{whisker} = \frac{l_{whisker}-(r_{whisker}-r_{anode})}{\kappa_{Au/Ni}\left(\frac{1}{2}(T_{-1}+T_{-2})\right)\pi r_{whisker}^2} + \frac{r_{whisker}-r_{anode}}{\kappa_{Au/Ni}\left(\frac{1}{2}(T_{-1}+T_{-2})\right)\frac{1}{2}\pi\left[r_{anode}^2+r_{whisker}^2\right]} \tag{E.3}$$

$$R_{hs1} = \frac{1}{4\kappa_{Au/Be/Cu}\left(\frac{1}{2}(T_{ambient}+T_{-1})\right)r_{whisker}} \tag{E.4}$$

$$R_{active,\,half2} = \frac{\frac{1}{2}t_{active}}{\kappa_{GaAs}\left(N_{D,\,active}, \frac{1}{2}(T_{4}+T_{5})\right)\pi r_{anode}^2} \tag{E.5}$$

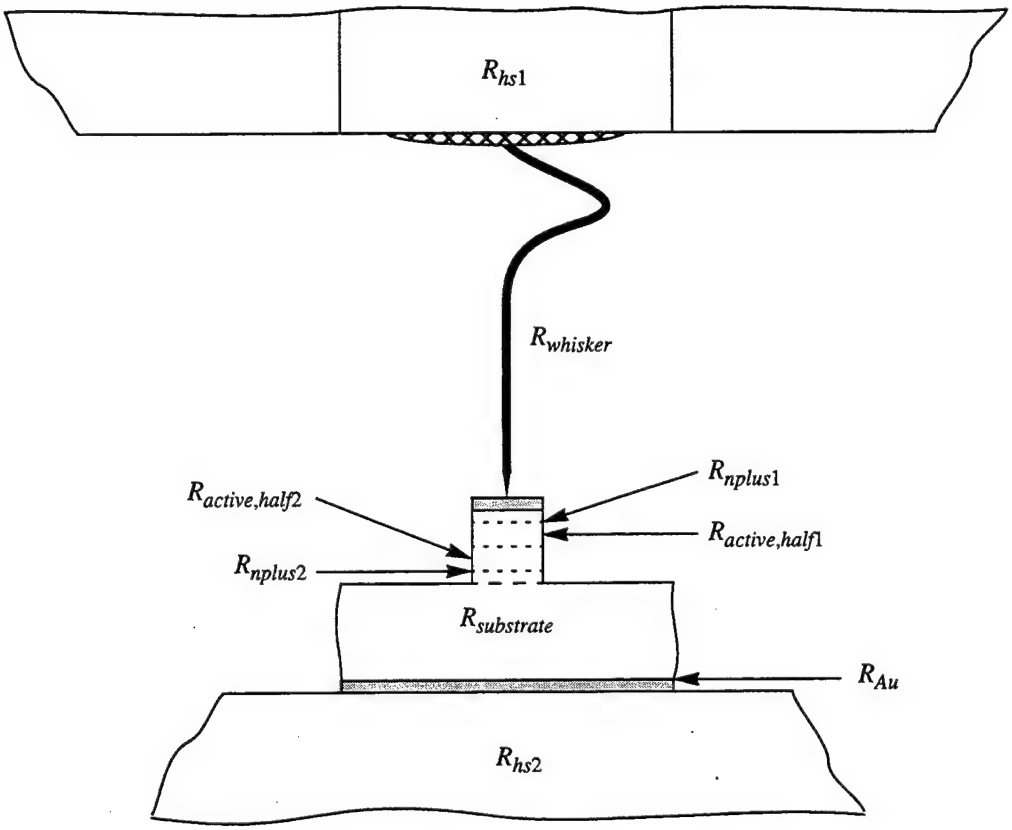

Figure E.1 Representative whisker-contacted geometry HBV multiplier circuit showing the geometry of Figure 4.5 and the constituent thermal resistance elements of Figure 4.7.

$$R_{nplus2} = \frac{t_{nplus2}}{\kappa_{GaAs}\left(N_{D,\,nplus2},\,\frac{1}{2}(T_3+T_4)\right)\pi r_{anode}^2}. \tag{E.6}$$

If $r_{chip} - r_{anode} \geq t_{substrate}$, the remaining thermal resistance expressions are

$$R_{substrate} = \frac{t_{substrate}}{\kappa_{GaAs}\left(N_{D,\,substrate},\,\frac{1}{2}(T_2+T_3)\right)\pi\left[\frac{1}{2}(r_{anode}+r_{anode}+t_{substrate})\right]^2}, \tag{E.7}$$

$$R_{Au} = \frac{t_{Au}}{\kappa_{Au}\pi\left[\frac{1}{2}(r_{anode}+t_{substrate}+r_{anode}+t_{substrate}+t_{Au})\right]^2}, \tag{E.8}$$

and

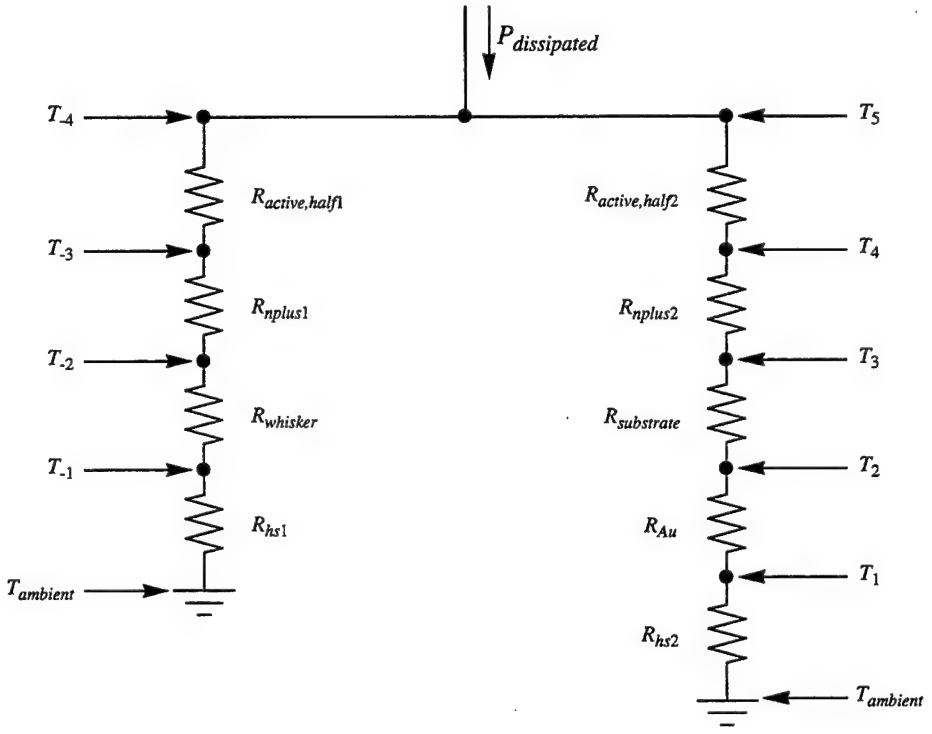

Figure E.2 Thermal resistance equivalent circuit for the representative whisker-contacted geometry HBV multiplier circuit of Figure E.1 showing the temperature designations at the constituent element boundaries.

$$R_{hs2} = \frac{1}{4\kappa_{hs2}(r_{anode} + t_{substrate} + t_{Au})}; \tag{E.9}$$

otherwise, the remaining expressions are

$$R_{substrate} = \frac{r_{chip} - r_{anode}}{\kappa_{GaAs}\left(N_{D,substrate}, \frac{1}{2}(T_2 + T_3)\right)\pi\left[\frac{1}{2}(r_{anode} + r_{anode} + t_{substrate})\right]^2} + \frac{t_{substrate} - (r_{chip} - r_{anode})}{\kappa_{GaAs}\left(N_{D,substrate}, \frac{1}{2}(T_2 + T_3)\right)\pi r_{chip}^2}, \tag{E.10}$$

$$R_{Au} = \frac{t_{Au}}{\kappa_{Au}\pi r_{chip}^2}, \tag{E.11}$$

and

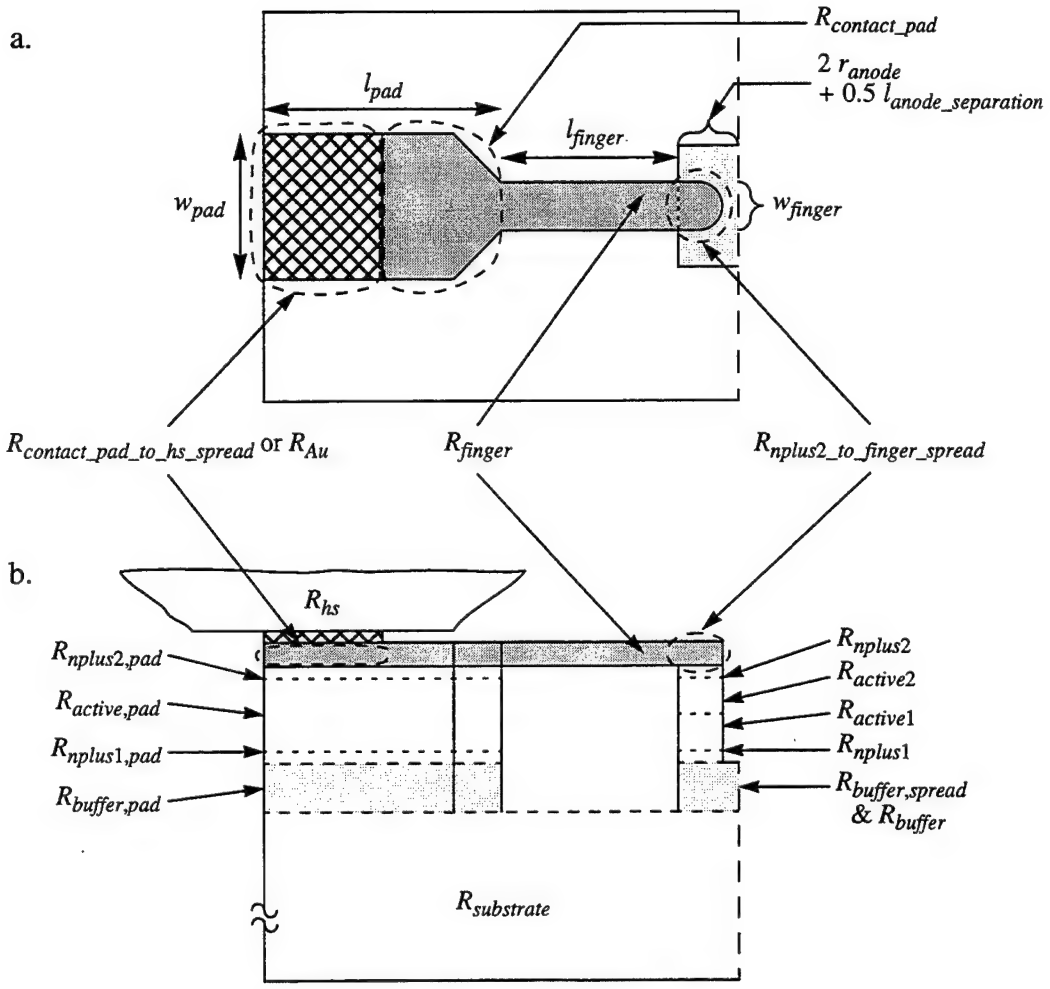

Figure E.3 Top (a.) and cross-sectional (b.) views of a representative planar geometry HBV multiplier circuit showing half of the geometry of Figure 4.6 and the constituent thermal resistance elements for half of Figure 4.8.

$$R_{hs2} = \frac{1}{4\kappa_{hs2} r_{chip}}. \tag{E.12}$$

E.2 Thermal Resistances of Planar Geometry HBV Frequency Multiplier Circuits

The thermal resistance expressions for whisker-contacted geometry HBV frequency multiplier circuits are given, in reference to Figures E.3 and E.4, by:

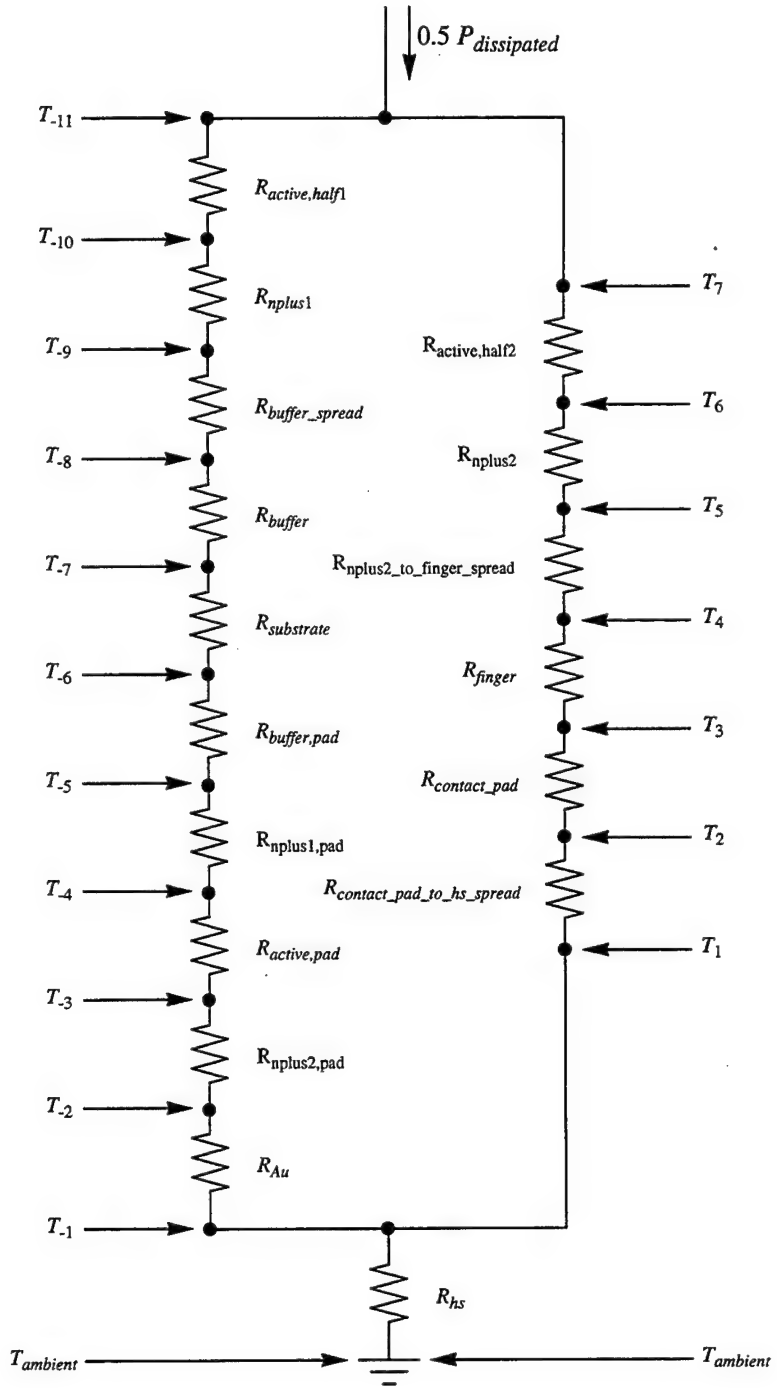

Figure E.4 Thermal resistance equivalent circuit for the representative planar geometry HBV multiplier circuit of Figure E.3 showing the temperature designations at the constituent element boundaries.

$$R_{active,\,half1} = \frac{\frac{1}{2}t_{active}}{\kappa_{GaAs}\left(N_{D,\,active},\frac{1}{2}(T_{-10}+T_{-11})\right)\pi r_{anode}^2} \tag{E.13}$$

$$R_{nplus1} = \frac{t_{nplus1}}{\kappa_{GaAs}\left(N_{D,\,nplus1},\frac{1}{2}(T_{-9}+T_{-10})\right)\pi r_{anode}^2} \tag{E.14}$$

$$R_{buffer\_spread} = \frac{\frac{1}{2}l_{anode\_separation}}{\kappa_{GaAs}\left(N_{D,\,buffer},\frac{1}{2}(T_{-8}+T_{-9})\right)\left(\frac{1}{2}(A_1+A_2)\right)} \tag{E.15}$$

$$R_{buffer} = \frac{t_{buffer}-\frac{1}{2}l_{anode\_separation}}{\kappa_{GaAs}\left(N_{D,\,buffer},\frac{1}{2}(T_{-7}+T_{-8})\right)\left(\frac{1}{2}(A_2+A_3)\right)} \tag{E.16}$$

$$R_{buffer,pad} = \frac{t_{buffer}}{\kappa_{GaAs}\left(N_{D,\,buffer},\frac{1}{2}(T_{-5}+T_{-6})\right)\left(\frac{1}{2}l_{pad}w_{pad}\right)} \tag{E.17}$$

$$R_{nplus1,pad} = \frac{t_{nplus1}}{\kappa_{GaAs}\left(N_{D,\,nplus1},\frac{1}{2}(T_{-4}+T_{-5})\right)\left(\frac{1}{2}l_{pad}w_{pad}\right)} \tag{E.18}$$

$$R_{active,pad} = \frac{t_{active}}{\kappa_{GaAs}\left(N_{D,\,active},\frac{1}{2}(T_{-3}+T_{-4})\right)\left(\frac{1}{2}l_{pad}w_{pad}\right)} \tag{E.19}$$

$$R_{nplus2,pad} = \frac{t_{nplus2}}{\kappa_{GaAs}\left(N_{D,\,nplus2},\frac{1}{2}(T_{-2}+T_{-3})\right)\left(\frac{1}{2}l_{pad}w_{pad}\right)} \tag{E.20}$$

$$R_{Au} = \frac{t_{finger}}{\kappa_{Au}\left(\frac{1}{2}l_{pad}w_{pad}\right)} \tag{E.21}$$

$$R_{active,\,half2} = \frac{\frac{1}{2}t_{active}}{\kappa_{GaAs}\left(N_{D,\,active},\frac{1}{2}(T_6+T_7)\right)\pi r_{anode}^2} \tag{E.22}$$

$$R_{nplus2} = \frac{t_{nplus2}}{\kappa_{GaAs}\left(N_{D,\,nplus2},\frac{1}{2}(T_5+T_6)\right)\pi r_{anode}^2} \tag{E.23}$$

$$R_{nplus2\_to\_finger\_spread} = \frac{r_{anode}+\frac{1}{2}t_{finger}}{\kappa_{Au}\left[\frac{1}{2}(t_{finger}w_{finger}+\pi r_{anode}^2)\right]} \tag{E.24}$$

$$R_{finger} = \frac{l_{finger}}{\kappa_{Au} w_{finger} t_{finger}} \tag{E.25}$$

$$R_{contact\_pad} = \frac{\frac{1}{2}(w_{pad} - w_{finger})}{\kappa_{Au} t_{finger}\left[\frac{1}{2}(w_{finger} + w_{pad})\right]} + \frac{\frac{1}{2} l_{pad} - \frac{1}{2}(w_{pad} - w_{finger})}{\kappa_{Au} t_{finger} w_{pad}} \tag{E.26}$$

$$R_{contact\_pad\_to\_hs\_spread} = \frac{\frac{1}{2}\left(t_{finger} + \frac{1}{2} l_{pad}\right)}{\kappa_{Au} w_{pad}\left[\frac{1}{2}\left(t_{finger} + \frac{1}{2} l_{pad}\right)\right]} \tag{E.27}$$

$$R_{hs} = \frac{1}{4\kappa_{hs}\sqrt{\frac{\frac{1}{2} l_{pad} w_{pad}}{\pi}}}. \tag{E.28}$$

The areas A_1, A_2, and A_3 (see Figure E.5) are given by

$$A_1 = \pi r_{anode}^2, \tag{E.29}$$

$$A_2 = \pi r_{A2}^2 - r_{A2}^2 \operatorname{acos}\left(\frac{r_{A2} - \frac{1}{2} l_{anode\_separation}}{r_{A2}}\right) + \left(r_{A2} - \frac{1}{2} l_{anode\_separation}\right)\sqrt{2 r_{A2}\left(\frac{1}{2} l_{anode\_separation}\right) - \left(\frac{1}{2} l_{anode\_separation}\right)^2}, \tag{E.30}$$

and

$$A_3 = \pi r_{A3}^2 - r_{A3}^2 \operatorname{acos}\left(\frac{r_{A3} - l_{A3}}{r_{A3}}\right) + (r_{A3} - l_{A3})\sqrt{2 r_{A3} l_{A3} - l_{A3}^2} - r_{A3}^2 \operatorname{acos}\left(\frac{r_{A3} - t_{buffer}}{r_{A3}}\right) + (r_{A3} - t_{buffer})\sqrt{2 r_{A3} t_{buffer} - t_{buffer}^2} \tag{E.31}$$

where

$$r_{A2} = r_{anode} + \frac{1}{2} l_{anode\_separation}, \tag{E.32}$$

$$r_{A3} = r_{anode} + t_{buffer}, \tag{E.33}$$

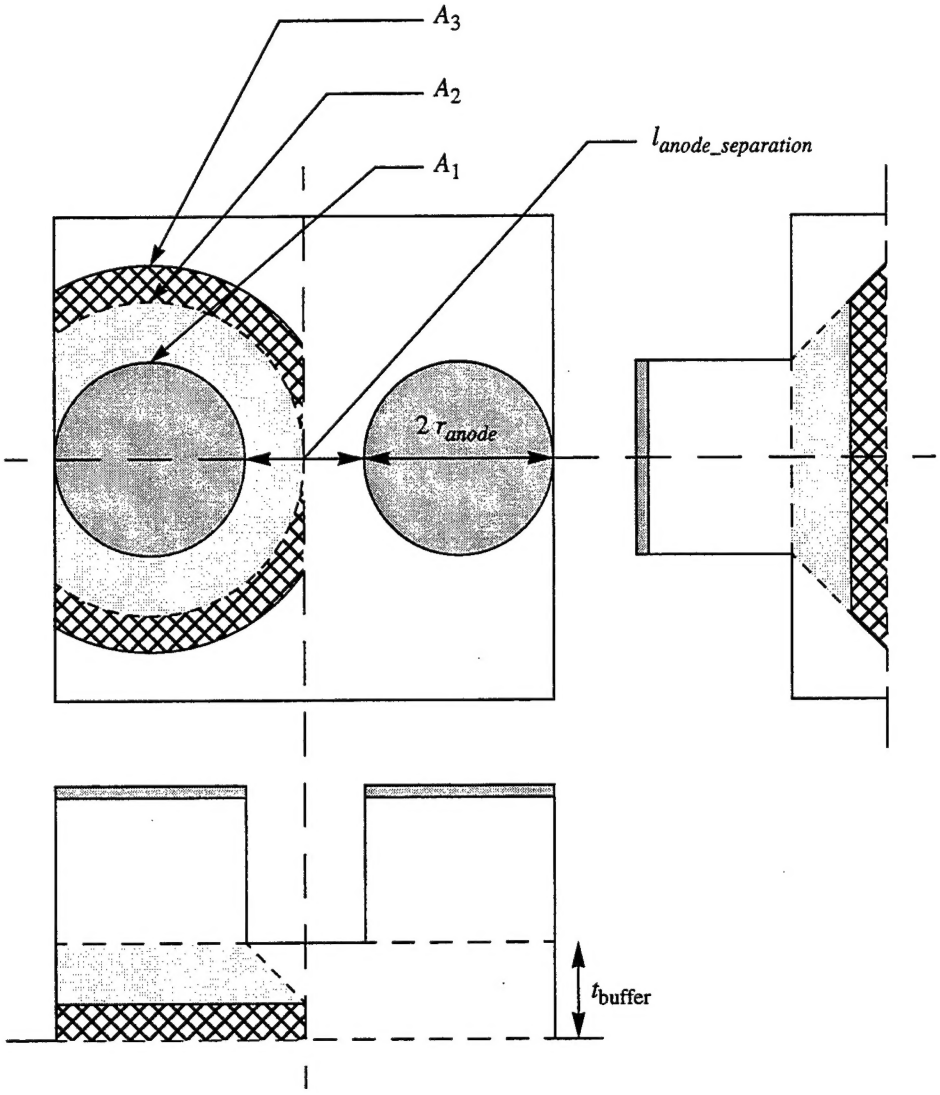

Figure E.5 Close-up top and cross-sectional views of anode mesa region for the representative planar geometry HBV multiplier circuit of Figure E.3 showing heat flow areas used in the thermal resistance calculations.

and

$$l_{A3} = t_{buffer} - \frac{1}{2} l_{anode\_separation}. \tag{E.34}$$

Finally, the planar geometry substrate thermal resistance, $R_{substrate}$, is calculated using the results shown in Figure 4.4. Again, this figure was generated using a three-

dimensional finite-element heat flow analysis program[E.1] to account for the substrate's irregular heat flow geometry. Using an input heat flow "port" width w_2 (see Figure 4.1d) calculated from

$$w_2 = \frac{\frac{1}{2}A_3}{l_2}, \tag{E.35}$$

the substrate thermal resistance is found by interpolating between the thermal resistance values for $w_2 = 5$ μm and $w_2 = 10$ μm at a given value of substrate thermal conductivity.

Appendix E References

[E.1] ABAQUS, Hibbitt, Karlsson, & Sorensen, Inc.

Vita

J. Robert Jones was born on January 19, 1968 in Trenton, New Jersey. He received the B.S. and M.S. degrees in electrical engineering from the University of Virginia, Charlottesville, Virginia, in 1990 and 1992, respectively.

From 1989 to 1995, he was a research assistant in the Semiconductor Device Laboratory at the University of Virginia where his research interests included semiconductor heterostructure device physics and modelling, nonlinear microwave and millimeter wave circuit analysis and design, and solid-state device fabrication. In December of 1995, he joined the technical staff of Anadigics, Inc. in Warren, New Jersey as a senior engineer.

He is a member of the IEEE (S'89, M'96), Tau Beta Pi, and Eta Kappa Nu.